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MAY 31, 1984

WORLDWIDE PUSH IS ON FOR HIGH-LEVEL NETWORK STANDARDS/78

New processes help bipolar hold its own against C-MOS/95

Denser boards demand multichip packages for SSI and MSI/103

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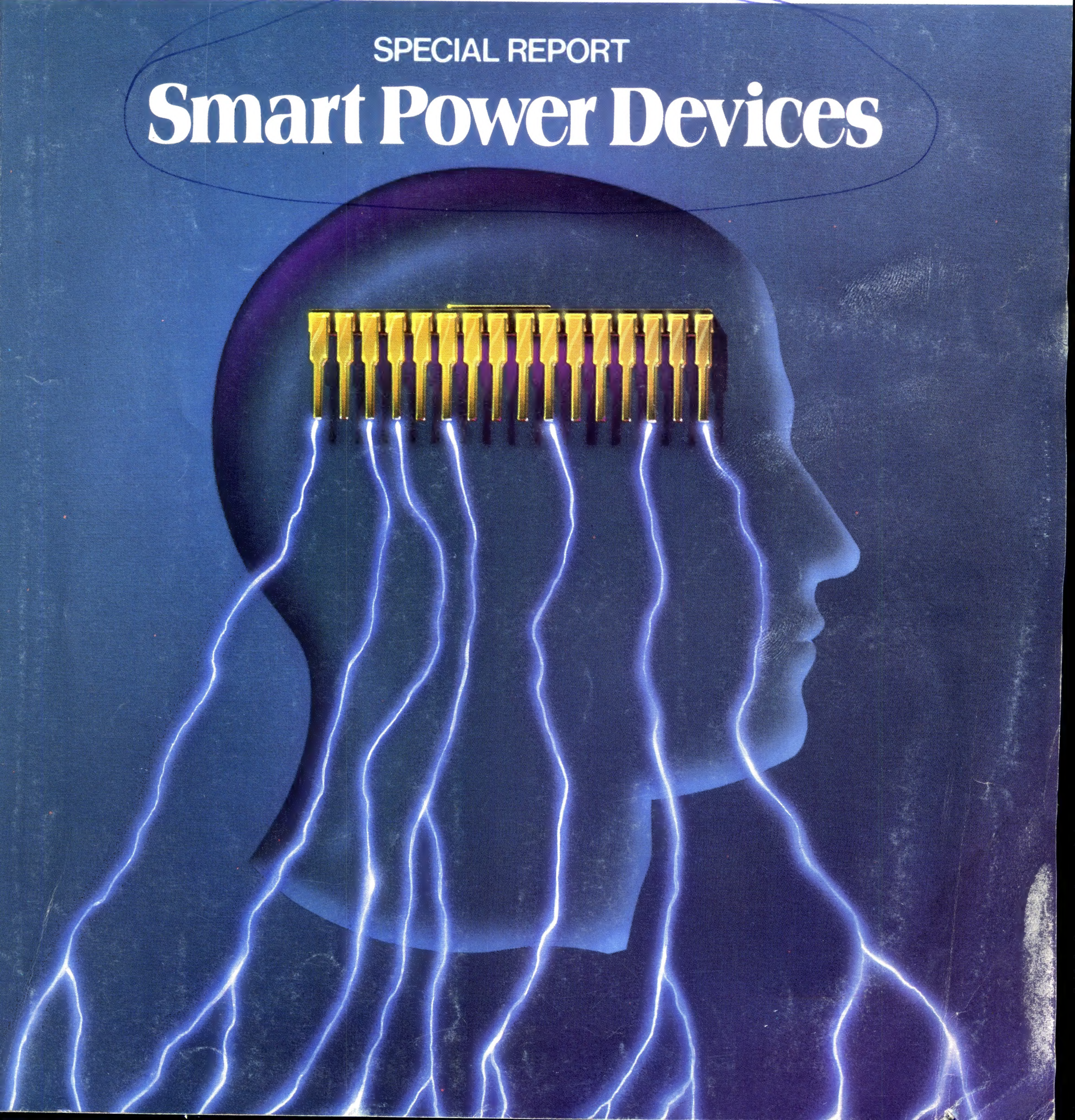
SPECIAL REPORT

Smart Power Devices



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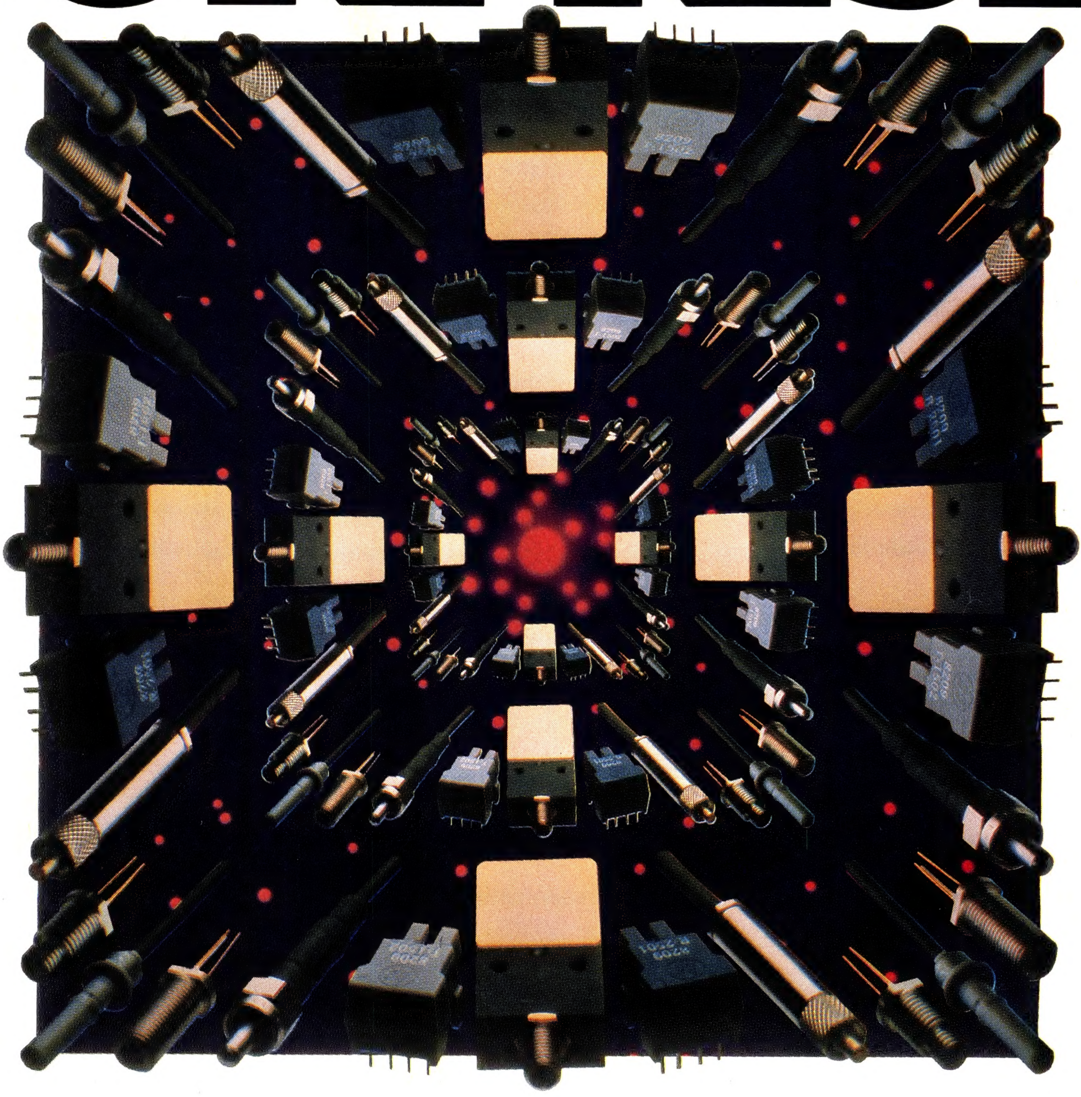

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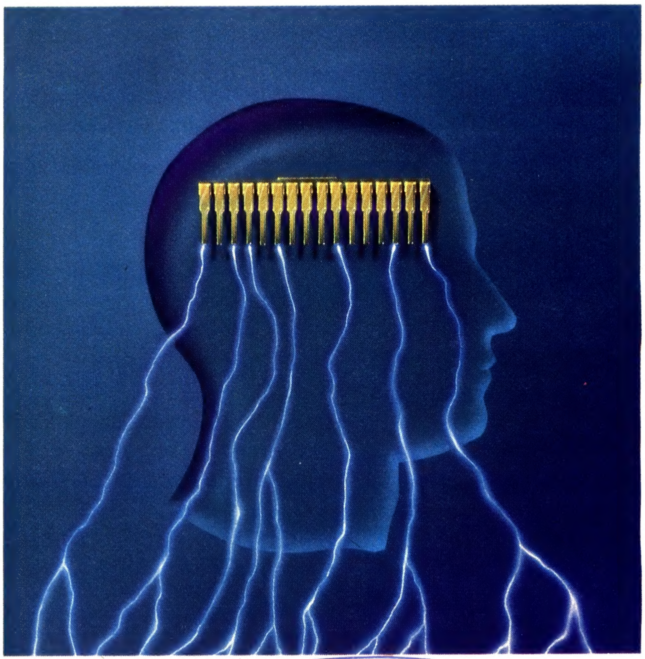

The Cover Story

Smart power devices

Combining high-power devices *on the same chip with low-voltage logic and control circuits, the burgeoning field of smart-power technology portends a revolution in circuit and system design*

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Highlights

Deregulation opens the doors wide for fm subcarriers, 75

The Federal Communications Commission leaves no spectrum unturned in its zest for deregulation—just look at what has happened to fm subcarriers. Their potential, the result of a series of deregulatory decisions, extends now from traditional applications such as background music to nonbroadcast services such as paging.

Work progresses on high-level local-net protocols, 77

Two big local-network demonstrations at the National Computer Conference scheduled for July 9-12 will use lower-level open-systems-interconnnection protocols to make heterogeneous machines talk to each other. Meanwhile, work is well under way around the world to produce high-level protocols—and the stakes are enormous.

C-MOS and TTL are likely to overlap in their digital-IC roles, 95

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CICC's broad focus centers on custom IC-design tools, 99

The Custom Integrated Circuits Conference, held last week, devoted much of its emphasis to custom integrated-circuit design tools, as well as to fabrication technology and applications. The conference addressed topics such as mixing bipolar and MOS technologies on a chip and electrostatic-discharge protection for MOS ICs. Two papers even focused on customized analog arrays, an important subject often untouched at such conferences.

What's ahead....

Worldwide semiconductor report:
A special report on the semiconductor business will examine the market's strength in the U. S., Western Europe, and Japan and will look at application-specific integrated circuits and distribution trends. . . . **June 14.**

256-K C-MOS RAMs:
An in-depth technical article will cover the development of a 256-K complementary-MOS dynamic random-access memory. . . . **June 14**

Computer graphics: This special report will look at the increasingly significant role of graphics in the latest computer systems. . . . **June 28.**

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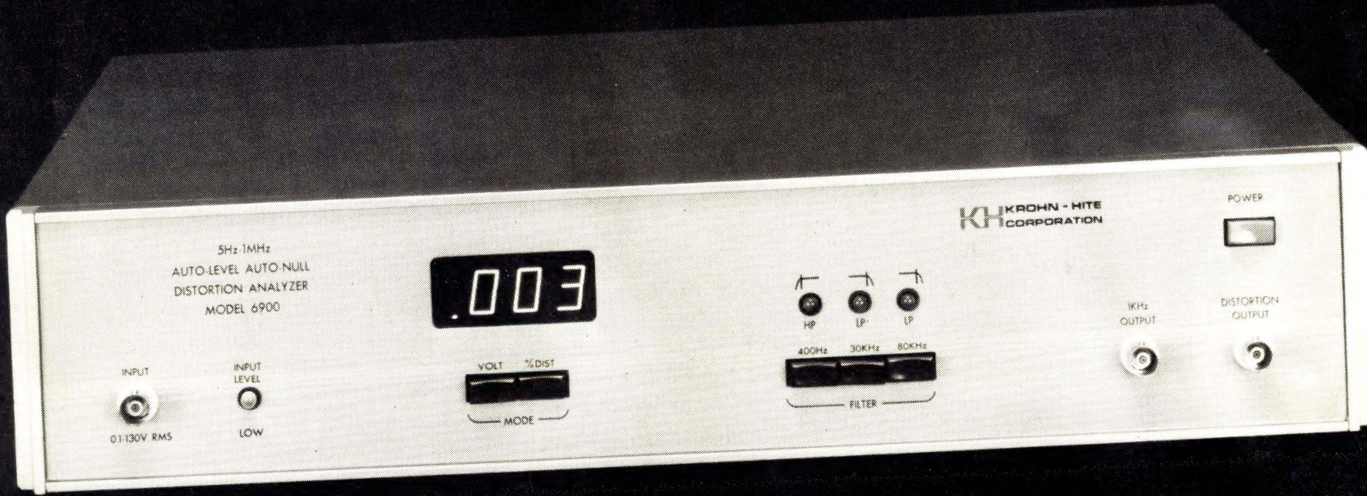

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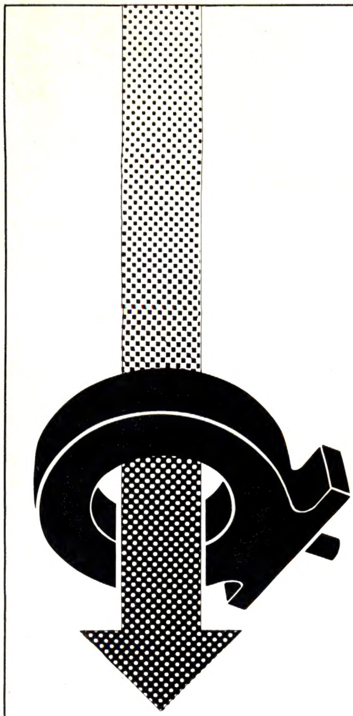

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Editor's letter

Making one's way to a convention in Las Vegas in any season calls for devotion to one's profession beyond measure or an unslaked thirst for knowledge bordering on obsession. Attending this year's National Computer Conference in July will require nothing short of heroism. Yet such determination may be well rewarded, according to Robert Rosenberg, our systems integration editor, who says that this year's NCC will feature landmark demonstations of just how far the industry has come in making possible the linking of computer hardware from different companies.

The demonstrations by General Motors Corp. and Boeing Co. will open the world's eyes to the power and the possibilities of the reference model for open-system interconnection, by which the world's computer makers hope to expedite the orderly growth of the industry by creating an open-system architecture. If the phenomenal growth of local networks is any indication, the establishment of such an architecture will have a profound impact on an already huge market.

Understanding this story calls for a knowledgeable guide through the thickets of competitive contention, political infighting, and technical subtleties inherent in any international standard development of such import, not to mention the need for wading through the "alphabet soup," as Bob refers to the myriad abbreviations and acronyms that infest the language of the standard makers.

In his "Inside the News" special report starting on page 78, he provides such a guide and also insight into the impressive efforts underway to bring all the world's diverse systems together under the OSI model. In a way, it is a tribute to the often thankless, difficult, and dedicated labor of hundreds of people working behind the scenes to forge the protocols and standards to achieve it.

It was inevitable that, after augmenting man's intellectual capacity beyond imagination, the electronic revolution should now address itself to heavy-duty power control. Technology has now solved some of the problems by putting logic circuitry and analog sensors on the same chip with *high*-current, high-voltage devices. This achievement now opens up whole new application areas, hence whole new markets.

As Ashok Bindra, our components editor puts it, the merger of logic and power on a single chip represents an unprecedented combination of electronic brain and brawn. Intrigued by the possibilities of this new partnership on a chip, Ashok began to gather material and talk to major participants in the technology three months ago. He ran into difficulty right away: although he found many companies heavily involved in development of what is being called smart power, only a few were willing to talk about their work in detail.

This was a sure sign that Ashok was on the trail of a timely story, so despite the reticence of many of the participants, he kept digging. The result is his special report and cover story starting on page 87.

Those who did open up to Ashok were unanimously enthusiastic about the potential of this new technology branch. One proponent, James E. Dykes, vice president and general manager of General Electric Co.'s Semiconductor division, sees the home as a major target for these new power-control chips.

Indeed, if you think about it, the typical home contains at least a dozen or more electric motors turning appliances on or off, rotating things, chopping them, mixing them, opening or closing them. What's more, there are countless other devices that heat and cool and control energy or use it in diverse ways. Each of these are potential mates for smart power chips that will improve efficiency or squeeze out more precision and permit greater optional control on the part of the homeowner.

And this doesn't even begin to estimate the possibilities of smart power in industrial process control, in automobiles and aircraft. Ashok believes we may very well be on the verge of another revolution as profound as that wrought by the microprocessor *itself.* □

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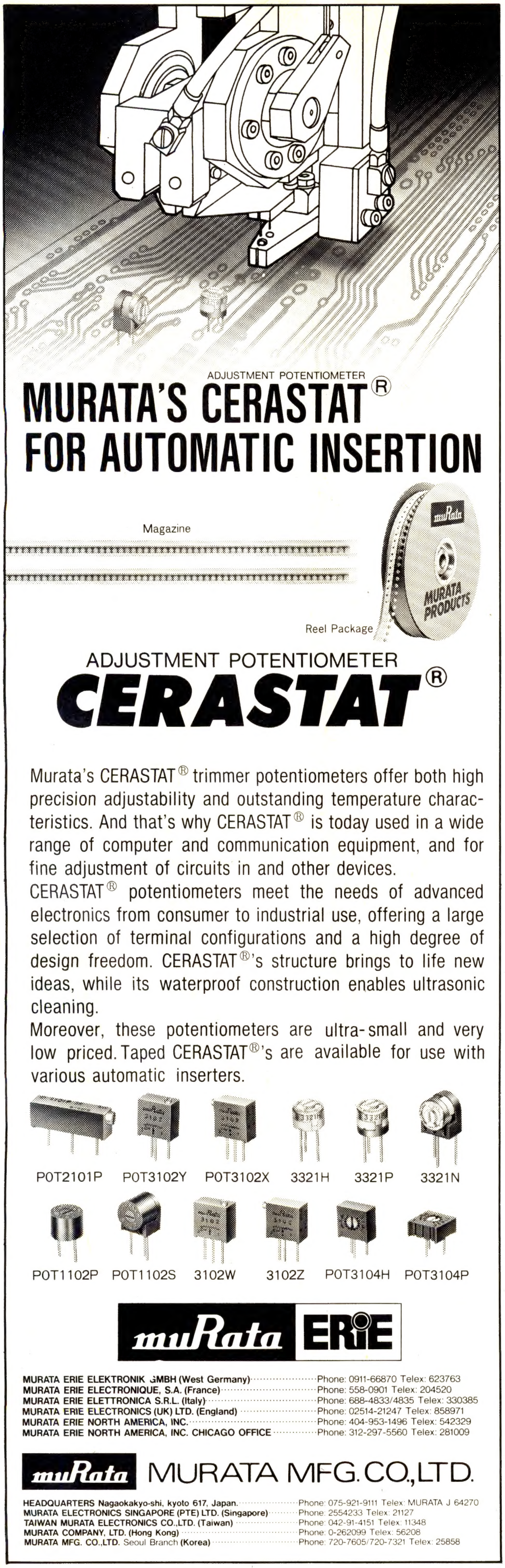
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Readers' comments

C is the worst

To the Editor: I could not disagree more with your article on the C programming language ("The power and the portability," April 19, p. 152). Why does "i+ =2" convey more information than "i=i+2"? It saves two characters, but so what—it just makes the code harder to read. C has other confusing operators, too. For instance, in some cases "&" indicates "address of"; in others, "bit-wise addition"; and in still others, "bit-wise intersection and increment."

In these days of constantly plunging memory costs, why don't we stop trying to save every last bit and start going back to the user interface and the human being it serves. Let's see programs written in English or its well-known derivative, the Basic programming language. It's readable, and compilers make it run faster than interpreters can. C is without doubt the worst language that I have ever had to work with.

The whole point of writing programs is twofold. First, we want to control the computer. Second, we want to be able to read the program back in the future, when we have forgotten it or when someone else wants to read it. We should therefore try to convey as much meaning as possible in each line of code instead of boiling the lines down to the point of unintelligibility. After all, a programmer's time is more expensive than memory.

Louis Schirm IV
DSP Systems Corp.
Anaheim, Calif.

Corrections

*In "Automate, emigrate, or evaporate," [*Electronics*, April 19, p. 101], the name of Maxtor Corp., of San Jose, Calif., was misspelled as "Maxstor Corp." And in the photograph on p. 104 of the May 3 issue ["Bay State firms ponder their future"], Richard Fidler, vice president and general manager of GTE Strategic Systems division, Westborough, Mass., was misidentified as Andrew Kariotis, president and chief executive of Alpha Industries Inc.*

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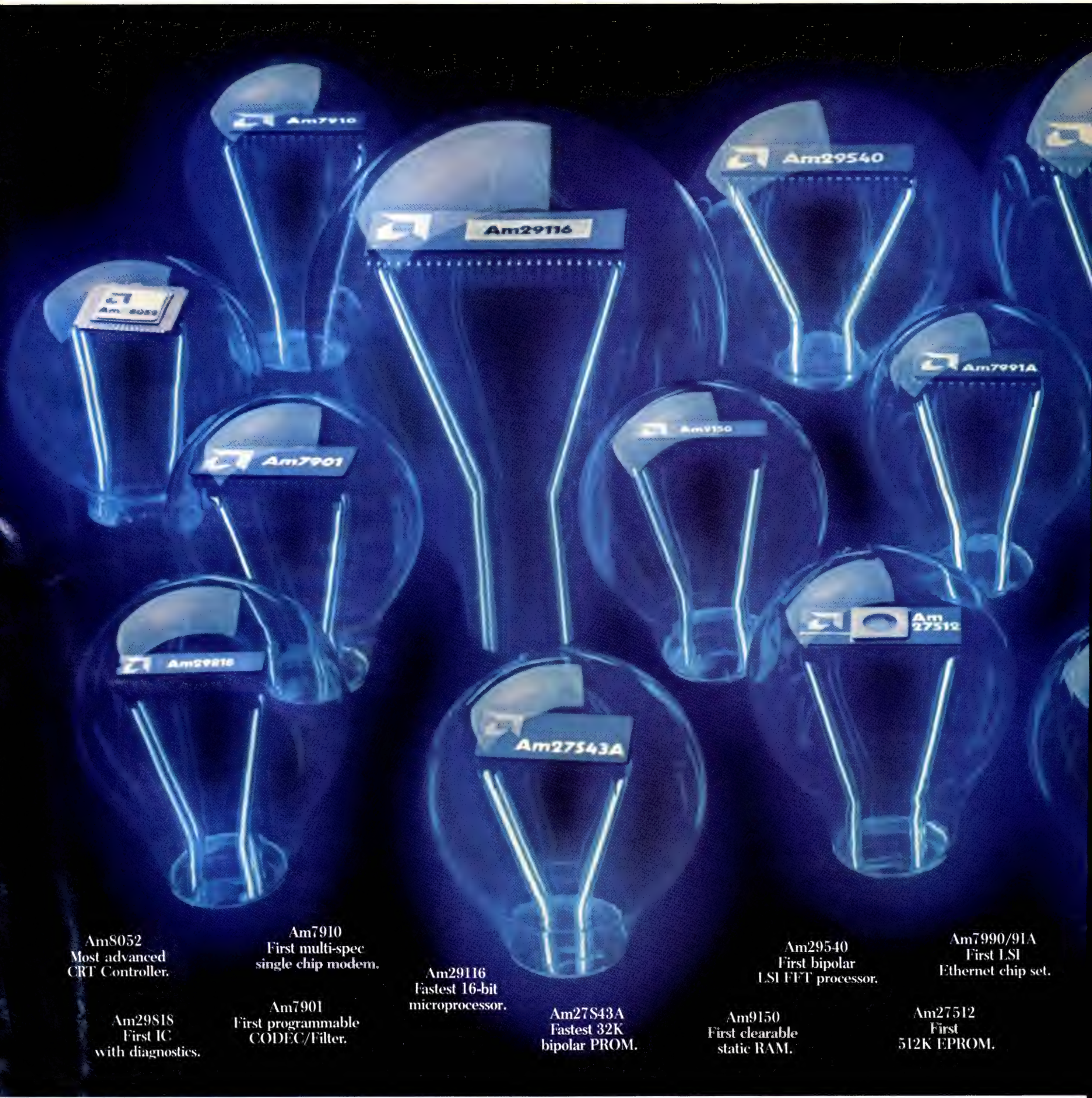

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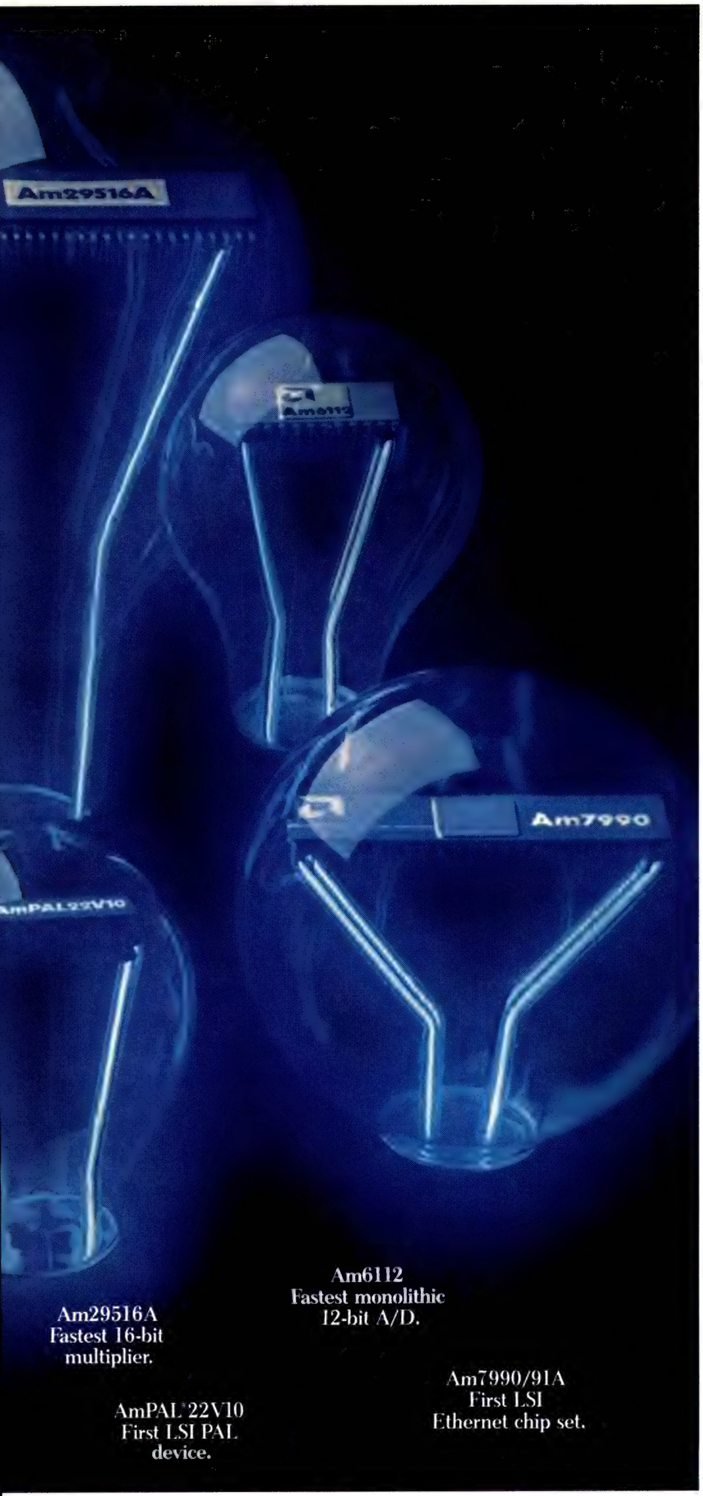

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High technology may not be the unemployment panacea

Trends, like so many things in these fast-moving times, do not last as long as they used to. It seems only yesterday that high technology was being hailed as the savior of Western civilization in general and the U. S. economy in particular. Therefore, advances in fields such as robotics and other electronics technologies were going to bring more jobs, prosperity, and a better way of life. Computers were the path and computer literacy the light, so students at every level were bombarded with the message, "Get into computers."

Now, however, it may be time for a second look.

It is beginning to appear that in the hot flush of discovery, not enough attention was paid to the fact that the proliferation of the computer and its cousin, the robot, is not going to create that many new jobs. Indeed, a good many will be eliminated and other problems will be created in the workplace (see p. 58).

Take, for example, a new study by Russell W. Rumberger and Henry M. Levin at Stanford University's Institute for Research on Educational Finance and Governance. It draws on the Bureau of Labor Statistics' projections of the U. S. labor market to 1995 and on similar analyses by the National Science Foundation and the Institute for Economic Analysis, an independent organization, and its conclusions, in light of the rosy predictions that have been made for high technology, are sobering. Among them:

- Less than 6% of all new jobs will be in high-technology applications.
- None of the 10 occupations with the largest expected growth in new jobs is related to high technology, and only two—teaching and nursing—require any education beyond secondary school.
- Earnings of the workers in those 10 occupations, such as cashier, general clerk, and secretary, were 30% below the national average in 1979.
- Between now and 1995, the U. S. may have 14 times as many new jobs for building custodians (779,000) as for computer service technicians (53,000).

Of course, the projections could be wrong. However, in the event that they are not, it is time for this country's educational establishment to take a hard look at what it has been telling itself—and the young people concentrating on science and engineering curriculums—about what is waiting a decade or so down the road.

Wanted: a lock and chain for floppy disks

Speaking of jobs created by computers, at least thieves of every stripe, from white collar to no collar, have seen the opportunities offered and seized them. The latest example, reported by the Associated Press, concerns a disk stolen from a booth at the convention of the American Institute of Architects, in Phoenix, Ariz. It seems the $2.50 floppy contained computer-graphics data valued by its disconsolate owner at upwards of $2 million. All of which suggests still another can't-miss money-maker: design a lock and chain that can keep a floppy disk at its owner's computer.

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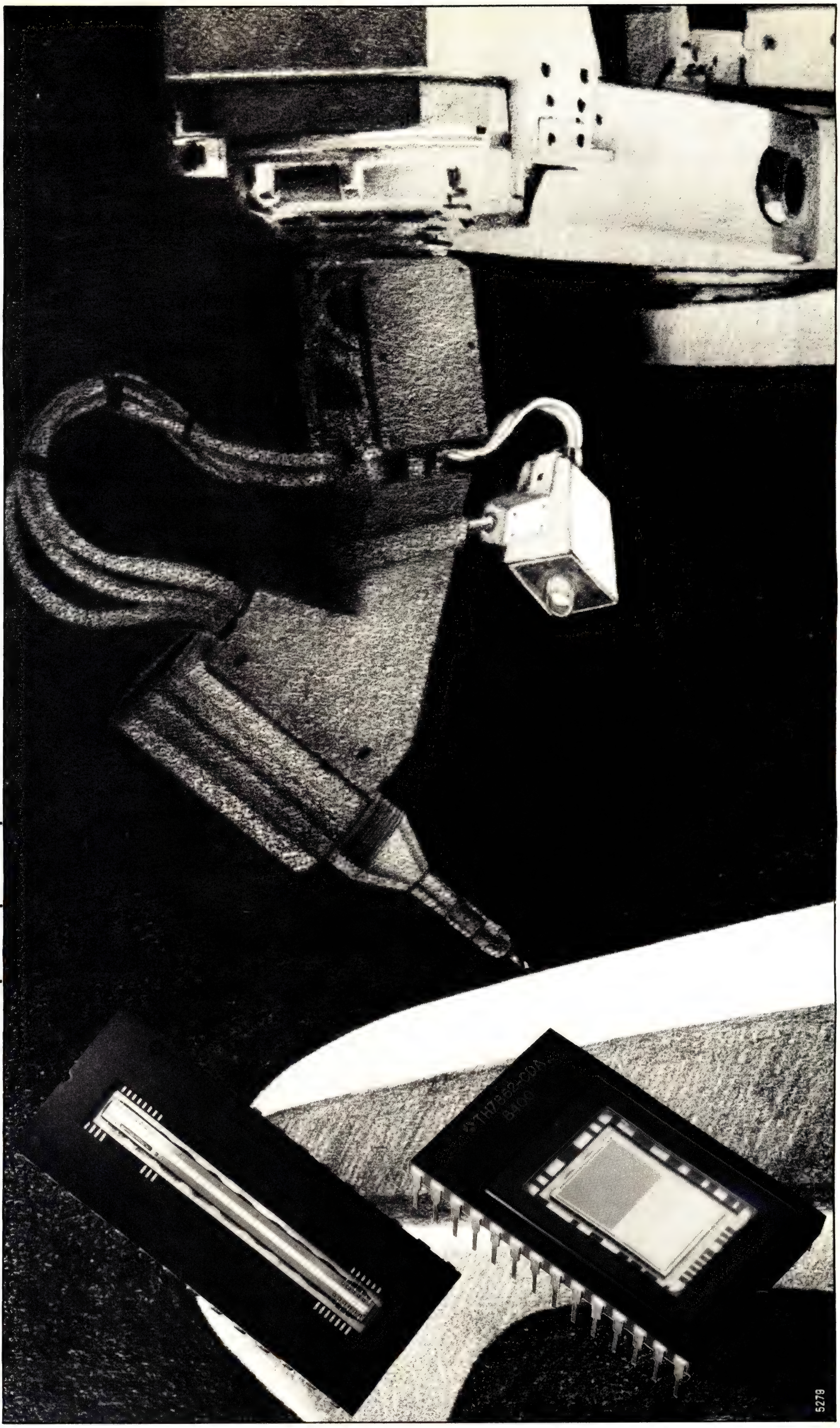

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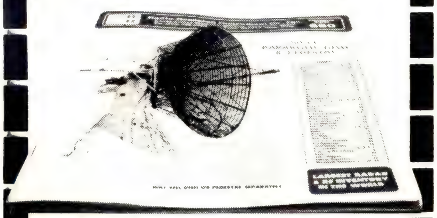

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People

Peck moves in at Saber to give marketing direction

When the venture-capital firms behind Saber Technology Corp. saw that the fledgling company's high-performance work station for computer-aided design was nearing the end of development, they followed the standard practice for technology start-ups by replacing the initial top management with an outside executive familiar with the marketplace. Picked to head the San Jose, Calif., firm was Dennis M. Peck, 41, a veteran of 17 years with NCR Corp., most recently as general manager of its engineering and manufacturing facility in San Diego, Calif.

The next step. Dennis Peck, fresh from NCR, is taking Sabre from start-up to manufacturer status.

Peck replaced Saber's founder, Paul Magnuson, who also started Magnuson Computer Systems Inc., which competed for some years in the IBM-plug-compatible mainframe field. Magnuson had the experience and knowledge of design-automation tools to build a next-generation work station that is based on National Semiconductor Corp.'s 160032 microprocessor and includes a high-resolution screen. Once the system was designed, the investors looked around for a manager and found Peck. Magnuson supported the move and remains a majority stockholder.

Peck became chairman, president, and chief executive officer of Saber in February. So fast was the pace in his new post that he did not find a home in Silicon Valley for three months.

At NCR, Peck supervised design, manufacturing, and strategic planning for medium- and large-scale systems, including the development of NCR's 32-bit microprocessor chip set.

"It was a good time to leave NCR," Peck says; "the company is doing well, and the chip set and the computers that use it are selling well and meeting production goals." He adds: "San Diego set me up for an operation like Saber. The only difference is that instead of submitting plans to corporate headquarters, we have a few more managers here." He's talking about the investors, who keep close tabs on operations at their company.

Saber is still a place where computer designers work in jeans and T-shirts in the back room, while marketing personnel in tailored suits operate at desks out front. The process of changing from a start-up to a manufacturer has been difficult but manageable, Peck says. "Everyone believes in installing controls," he reports, "but it's like pulling teeth to get them working."

George does juggling act to help Motorola make ICs

New boom cycles in semiconductor sales may present a rosy outlook for the chip industry, but for wafer-fabrication managers, too much of a good thing offers some stiff challenges. For instance, preparation of advanced processing lines for new products must stay on schedule even as demand is met for maturing parts.

Such is the dilemma for William L. George, 41-year-old director of wafer-processing development at Motorola Inc.'s MOS operation in Austin, Texas. George is also Motorola's new worldwide strategic manager for MOS manufacturing.

"Everything that we build is in extremely high demand, and of course we believe that in the next downturn the more mature products will see a slackening of demand. But if we are poised properly with new products, the overall demand will hold up," says the Oklahoma native, named to his new position earlier this year after working as reliability and quality

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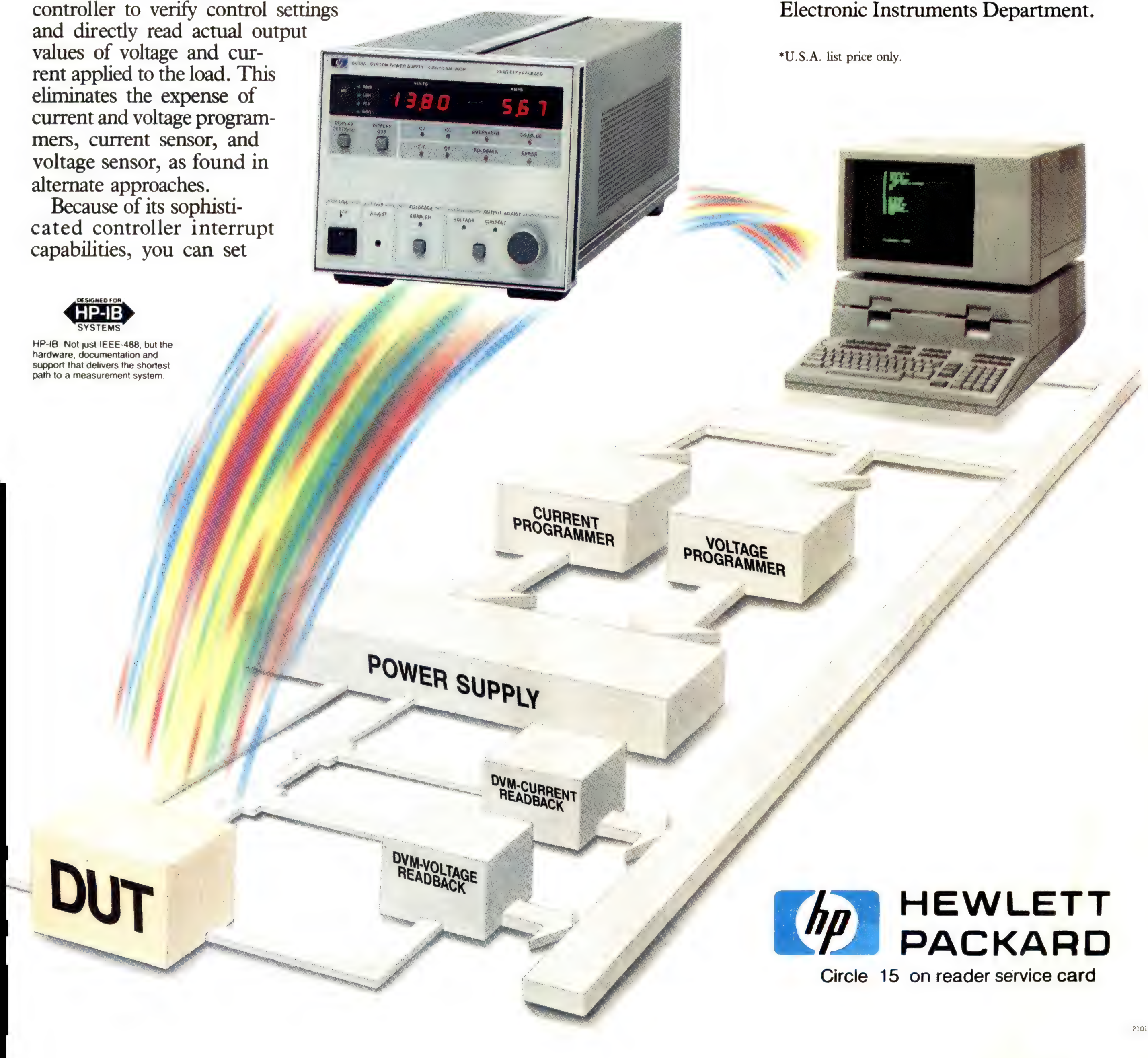

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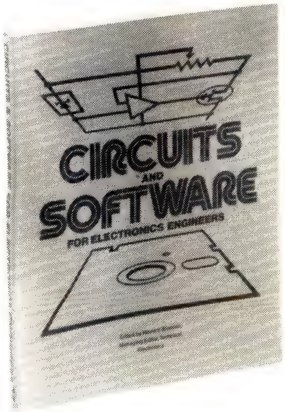

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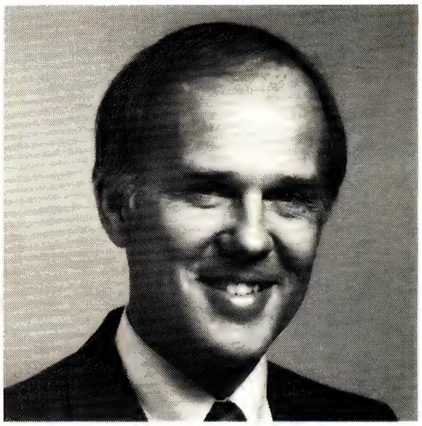

Looking ahead. William L. George sees automation gaining slowly in wafer fabrication.

assurance manager since 1980.

Before that, George had a decade of experience in wafer-fabrication processing, starting his career in 1968 with Motorola as a physicist in the Phoenix semiconductor research and development labs. Earlier that year, he completed his doctorate in material science at Purdue University. George had earned a BS in metallurgical engineering from the University of Oklahoma in 1964.

Motorola is now ramping up production at its most advanced complementary-MOS facility, known as MOS 8, in Austin. Chips can be produced there in high volumes with 1.5-to-2-micrometer geometries.

But today's wafer-fabrication manager is also faced with upgrading existing lines for the more advanced products, he adds. Moreover, for both new and existing lines, the logistics are no small potatoes.

Obtaining fabrication equipment is growing tougher, George notes, adding that equipment suppliers are also pressed by record demands. "Our suppliers are strapped, and since the beginning of the year it has been getting worse. We think it will continue," he says.

Higher levels of automation in selected suitable processes are now taking hold in the industry as one way to tighten control of the manufacturing processing, says George. "But it's not a blind jump into automation," he cautions. "Instead, it is now being aimed at selective automation of processes that can be done very quickly and realistically." ☐

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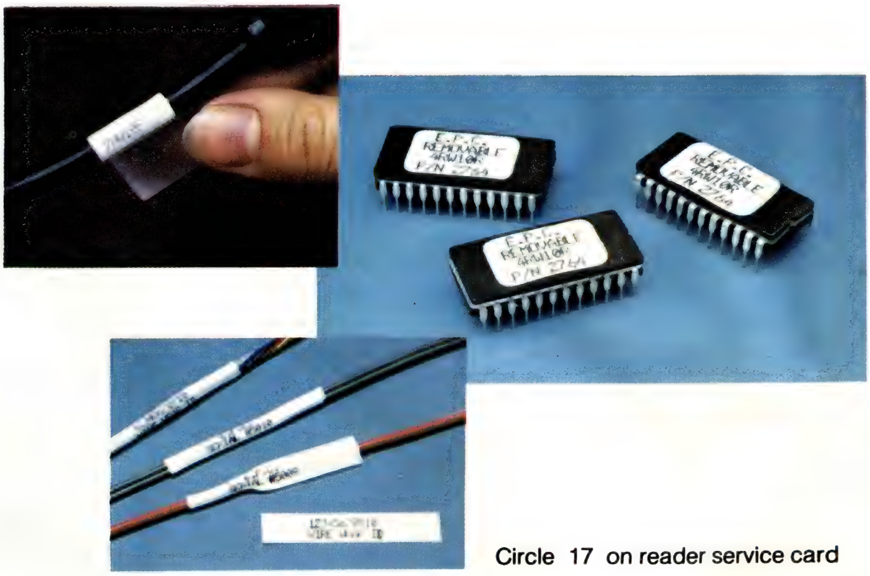

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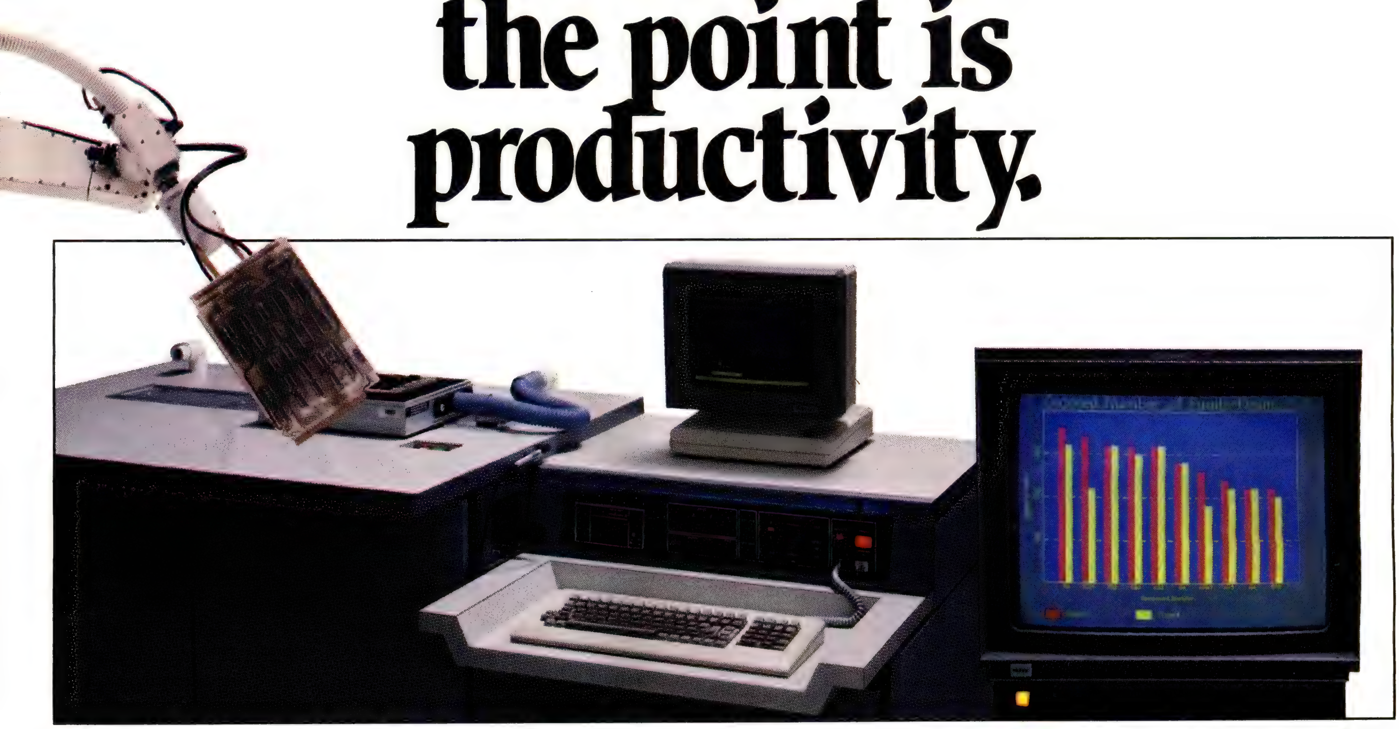

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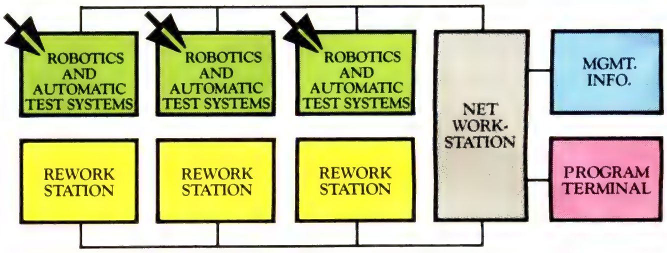

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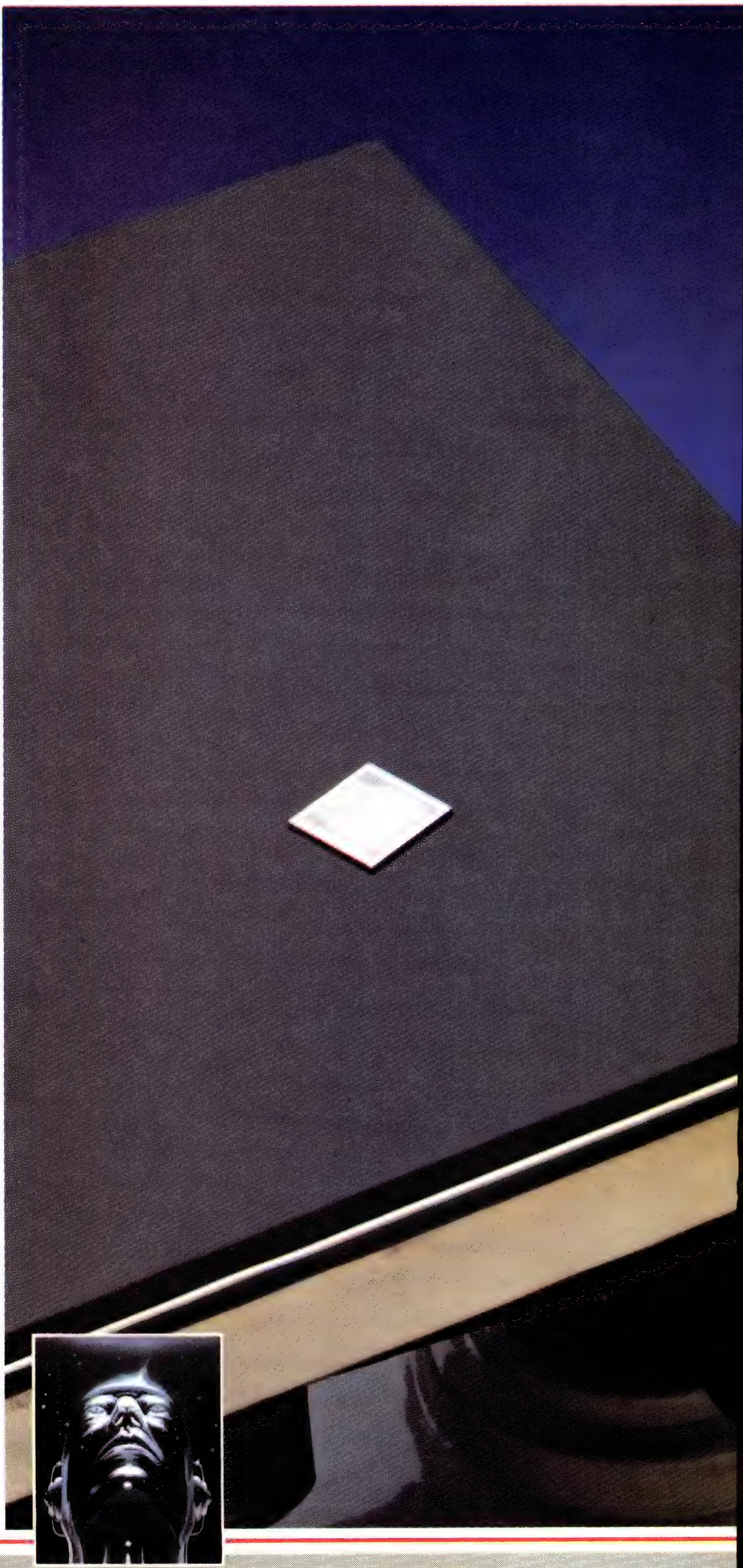

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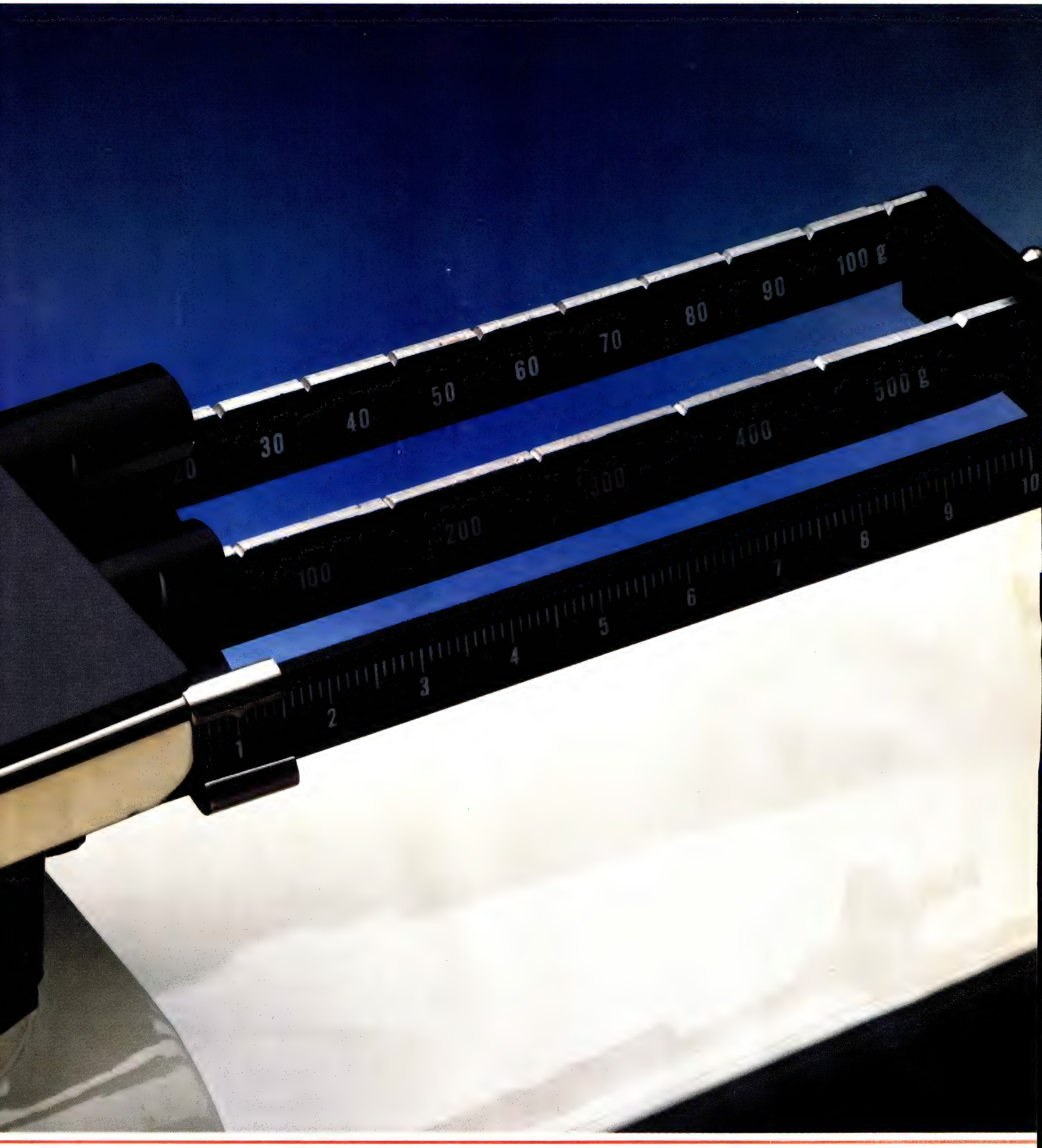

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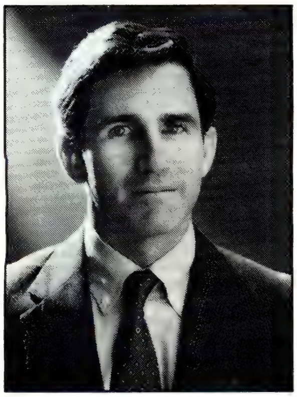


The strides being made in developing information technologies are as plain to the average American as the changes in telephones in homes and offices and the ads in newspapers. Yet the misapplication of new technology is almost as apparent: sophisticated telephone systems, word processors, computer networks, electronic mail, memory typewriters, and communicating telecopiers are generating more paper and more data but are not raising the productivity of our businesses proportionately—and productivity is a practical way to gauge progress.

What is missing? Why are technological miracles failing to produce results in the everyday world—helping us to work more productively, giving us a competitive edge? The answer lies with the basics: to influence productivity, data must be delivered as useful information into the hands of those who need it.

Two big shortcomings are blocking U. S. businesses from reaching this goal. They are deceptively simple—once the symptoms of the trouble are separated from the causes.

First, those who use technology are not taking the time to know themselves well enough before introducing new and powerful yet unfamiliar communications tools. In business, that means planning. The importance of information—who needs it, where, and when—must be known, and efforts to apply information technologies must be integrated into the business-planning process and into operations.

But today, with so many confusing alternatives and such great risks and rewards, most businesses still are failing to integrate communications planning into business planning. Three significant obstacles stand in the way:

- Too often, organizational placement of communications responsibilities is wrong. Voice and data communications and office automation are viewed as separate functions reporting to different senior executives. Strong, competent personnel may be lacking. Upper management's participation and visibility may be low.
- The perception—or rather misperception—of business communications and computers as necessary evils has given business-communications planning a low priority. The focus is on costs rather than benefits.
- Management has misplaced its expectations on cost justification in terms of potential return on investment—and wrong expectations inevitably lead to misconceptions about the benefits of communications. For instance, if management expects word processing to pay for itself by eliminating a secretary or two, then the expectation is misplaced. But if management perceives that word processing, by helping professional and clerical teams to generate more and better work in considerably less time, can substantially improve the company's image and competitive position—and hence, revenues and profits—then the ultimate benefits are in the bottom line and the equipment is truly cost-effective.

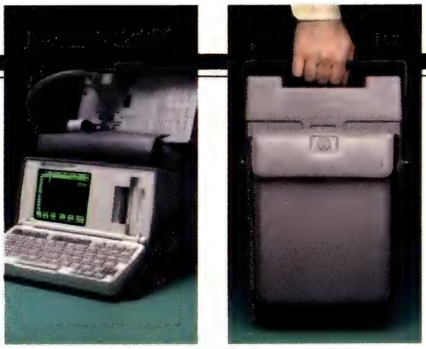
Priority needed. The second big shortcoming is the failure to make information-resources management, including communications, an executive priority. Progress cannot be made without executive awareness that there is a gap between existing communications technologies and the way they are currently used.

The choices among the dizzying array of telecommunications technologies will not be made properly without the direct participation of top management: where should the business be going and what information and communications support does that goal call for? Is there a possibility of locking the firm into a costly dinosaur that will not change with the times? Or is the company too frightened to install a system that may pay for itself quickly although it becomes outdated almost as fast?

These and other issues will be addressed by putting the business and telecommunications issues in their proper perspective and gaining the leadership of senior officers. Unlike the princess and frog of fable, today's miracles are not "passive"—not just picked up, kissed, and plunked down to work their magic. They require effort to gain a real payback in productivity.

On this page, Electronics *will periodically invite the expression of outside views concerning issues of importance to the electronics industries.*

HP introduces rugged portability in a high-performance protocol analyzer for only $3995*.



14.0 pounds of portability.

Now you can afford to apply high-level protocol analysis to your datacommunications problems, wherever they take you. Simply take along the new portable yet powerful HP 4951A Protocol Analyzer, and you'll have all you need to accurately diagnose and correct network operating problems. Simulate network components, monitor data transmission, perform bit error tests, and even do remote testing linked to a central HP 4955A Protocol Analyzer. Compare this price/performance to any other contender, and see why we call the HP 4951A the new standard for datacomm network field service.

The preferred choice for equipment manufacturers, service providers, and end users.

Network downtime is a costly proposition. With the low-cost HP 4951A, you can keep your network (or your customers' networks) operating at high efficiency. Sixty-three triggers give you extensive data analysis capabilities up to 19.2 kbps real time. In post-processing mode, you can do detailed repetitive analysis on those really hard-to-track errors. Trap on characters, error conditions, and lead transitions. BERT mode lets you measure bit errors, block errors, errored seconds, and percent error free seconds to quickly isolate problems down to the network component level. Plus you can simulate a CPU, modem, terminal, or group of terminals for complete interactive testing.

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Test programs written on the HP 4955A can be transferred to a remote HP 4951A and run without modification. Remote transfer of data, menus, timers, and counters is likewise a simple operation. This improvement gives field service personnel direct access to home office technical resources, for those really tough network problems.

To find out more about the HP 4951A Protocol Analyzer, or the HP 4955A Protocol Analyzer, call your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

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Meetings

PC Expo (333 Sylvan Ave., Englewood Cliffs, N. J. 07632), New York Coliseum, New York, June 26–28.

Government Computer Expo, U. S. Professional Development Institute (1620 Elton Rd., Silver Springs, Md. 20903), Sheraton Washington Hotel, Washington, D. C., June 26–28

European Computer Communications Conference and Exhibition, Online Conferences Ltd. (Networks 84, Online Conferences Ltd., Pinner Green House, Ash Hill Dr., Pinner HA5 2AE, Middlesex, England), Wembley Conference Centre, London, England, July 3–5.

Tesla Unconvention, Tesla (Peter Lefferts, 1640 Decker Ave., San Martin, Calif. 95046), Hill Country Convention Center, Morgan Hill, Calif., July 7.

Association for Women in Computing Third National Conference, Association for Women in Computing (AWCC 84, Patricia Timpanaro, 40 Main St. #206, Stoneham, Mass. 02180), Holiday Inn Center Strip, Las Vegas, Nev., July 8.

National Computer Conference, The American Federation of Information Processing Societies Inc. *et al.* (Marty Byrne, AFIPS, 1899 Preston White Dr., Reston, Va. 22091), Las Vagas Convention Center, Las Vegas, Nev., July 9–12.

10th International Liquid Crystal Conference, (Alan Mosley, Chief Scientist's Unit, Hirst Research Centre, GEC Research Laboratories, East Lane, Wembley HA9 7PP, Middlesex, England), University of York, July 16–20.

Office Automation/Information Systems Conference and Exposition, Association of Information Systems Professionals (1015 N. York Rd., Willow Grove, Pa. 19090), McCormick Place, Chicago Westin Hotel, Chicago, July 17–21.

Information Resources Integration, Engineering Foundation (345 E. 47th St., New York, N. Y. 10017), New England College, Henniker, N. H., July 22–27.

Summer Computer Simulation Conference, Simulation Councils Inc. (P. O. Box 2228, La Jolla, Calif. 92038), Copley Plaza Hotel, Boston, July 23–25.

Semicon/Osaka 84, Semiconductor Equipment and Materials Institute, Inc. (William F. Galarneau, SEMI, 625 Ellis St., Suite 212, Mountain View, Calif. 94043), Minato Fairground, Osaka, Japan, July 25–27.

Siggraph 84–11th Conference on Computer Graphics and Interactive Techniques, Association for Computing Machinery *et al.* (Richard Mueller, Control Data Corp., HQN 4QX, 8100 34th Ave. S., Bloomington, Minn. 55420), Minneapolis Auditorium and Convention Center, Minneapolis, Minn., July 25–29.

Seminars

Beyond System/34: IBM and Non-IBM Alternatives, TechTran (72 Cummings Point Rd., P. O. Box 10212, Stamford, Conn. 06904), St. Regis Sheraton Hotel, New York, N.Y., June 25–26.

Industrial Morphology, Machine Vision International Corp. (Pat Koschalk, Machine Vision International Corp., 325 E. Eisenhower, Ann Arbor, Mich. 48104), Sheraton University Inn, Ann Arbor, Mich., July 9–12.

Third IBM/Amdahl Users Computer Security Workshop, Computer Security Institute (Department IP, 43 Boston Post Rd., Northborough, Mass. 01532), Marriott Crystal Gateway, Washington, D. C., July 16–17.

Frequency Stability and Its Measurement, National Bureau of Standards (Mike Lombardi, Time and Frequency Division, NBS, 325 Broadway, Boulder, Colo. 80303), NBS Boulder Laboratories, Boulder, Colo., July 24–26.

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NEC NEWSCOPE

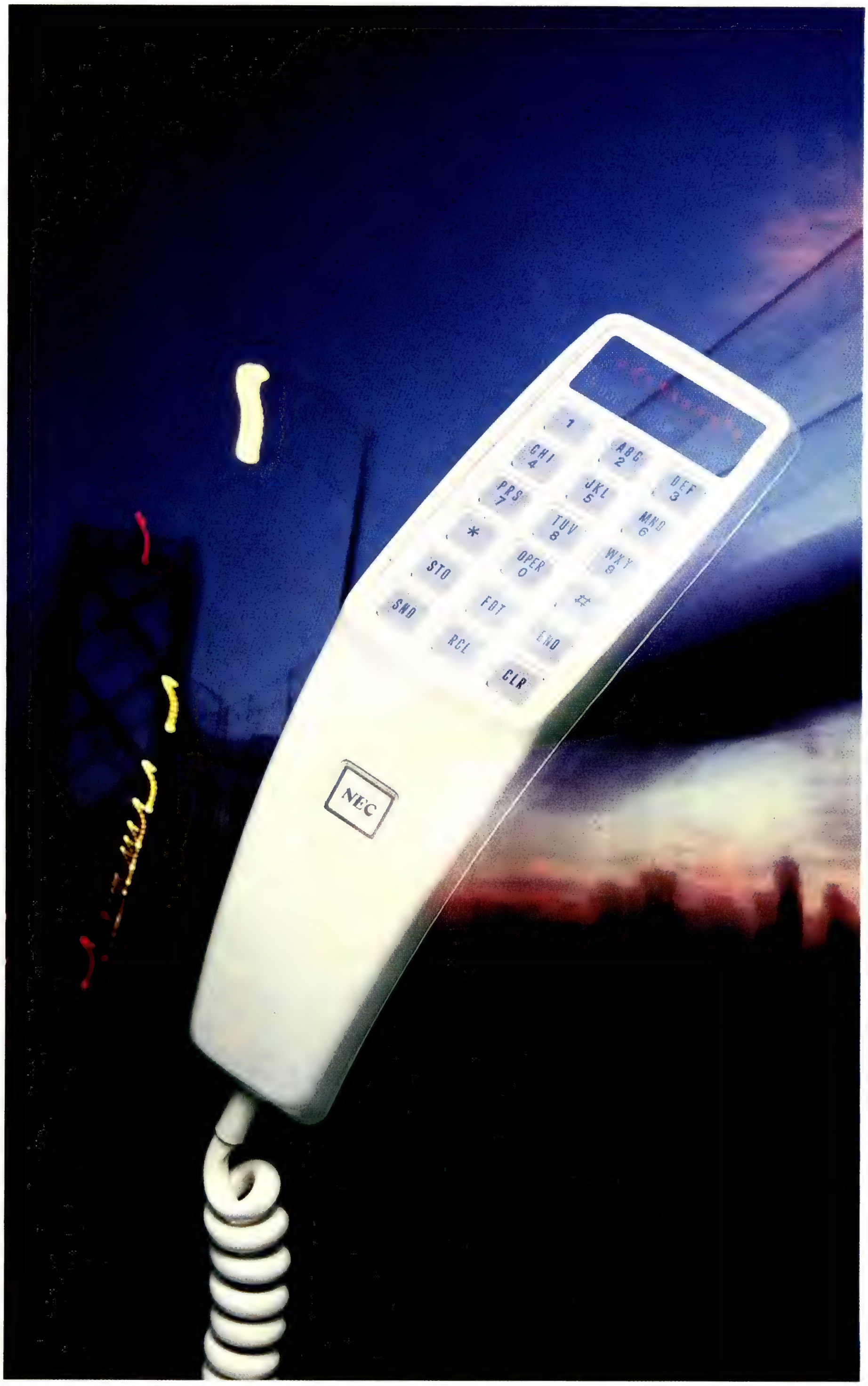
JORDAN MOVES UP TO CELLULAR MOBILE TELEPHONE

NEC will install an advanced cellular mobile phone system in Jordan by the end of 1984. The system will provide high-grade mobile telephone service in the 800MHz band. Initially, it will serve 1,500 subscribers in the capital and its suburbs (Greater Amman). It will have six mobile base stations (10 radio zones). Plans call for expansion to accommodate 10,000 subscribers with a network of mobile base stations covering the entire nation of Jordan.

A digital switching system will serve as the control center of the mobile telephone network. An MTS version of the renowned NEAX61 central office system will be used to interface the mobile service with the public switched telephone network. This interface will be handled through a tandem switching system.

NEC's Advanced Mobile Telephone System is a highly sophisticated cellular system integrating every type of equipment required for fully automatic mobile telephone service. It facilitates communications between vehicles and land subscribers and between vehicles.

NEC installed the world's first commercially operated cellular mobile telephone system in Tokyo. Other NEC cellular systems installed include an 800MHz system in Hong Kong, 400MHz systems in Mexico and Singapore and a 500MHz system in Australia.



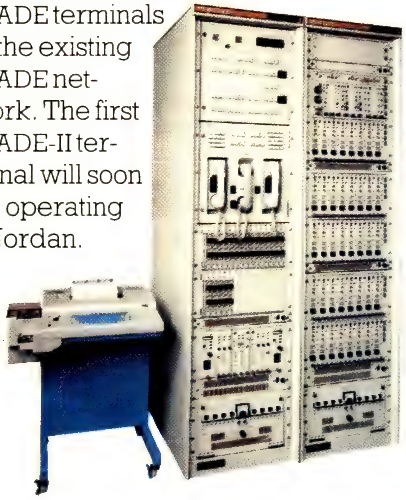
NUMBER 130

SPADE-II FOR INTELSAT ATLANTIC REGION

SPADE-II terminal equipment, designed to the latest INTELSAT SPADE Specification and completely compatible with existing SPADE terminals, will soon make its operational debut in the INTELSAT system, Atlantic Ocean Region. Incorporating state-of-the-art microprocessors and LSIs, it provides excellent reliability as well as simple operation.

The SPADE system allows a user to establish a communications circuit on demand with any other SPADE user, greatly improving satellite transponder utilization efficiency. It handles several times more telephone traffic using the same number of SCPC channel units. In addition, it considerably reduces annual operation cost because each SPADE circuit is billed not on a fixed annual rate but on an actual utilization basis.

NEC supplied 28 of the original SPADE terminals in the existing SPADE network. The first SPADE-II terminal will soon be operating in Jordan.



NEW LDR SYSTEM FOR BUSINESS COMMUNICATIONS

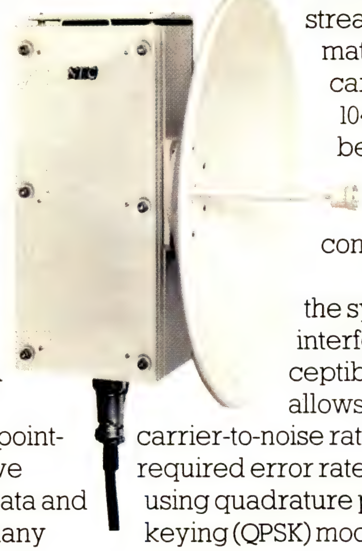
NEC now offers a highly sophisticated 10.5GHz digital local distribution radio (LDR) system. It meets the increasing need for low-cost, high-speed, and quality transmission of digital data for business communications.

NEC's 10.5GHz system, first put into operation in New York City, was developed as an advanced technological solution to local distribution problems. The system is based on a field-proven 2GHz LDR system using TDMA technology.

The new system provides point-to-multipoint digital microwave links for local distribution of data and voice from a node station to many subscribers with a single pair of radio frequencies. Each system covers a 90-degree sector with a radius of up to 15km. As many as 26 subscriber stations in each sector are served by one local node station. Radio frequency reuse in several quadrants can significantly increase the service range and maximize system flexibility.

The LDR system transmits up to twenty-six 56 or 64 kbps data or voice channels—a total bit stream of approximately 1.8 Mbps per carrier. As many as 104 subscribers can be accommodated by one node with a maximum configuration.

A key feature of the system is its low interference susceptibility. The system allows a very low carrier-to-noise ratio to obtain the required error rate performance by using quadrature phase shift keying (QPSK) modulation, thus enabling many frequencies (up to 20) to be used in the same area.



NEW 1,300nm LASER DIODES

NEC's new laser diodes feature our exclusive Double-Channel Planar Buried Heterostructure (DC-PBH). This feature improves efficiency and reduces the temperature dependence of the operating current. Double channel structure also minimizes crystalline defects to provide more stable operation.

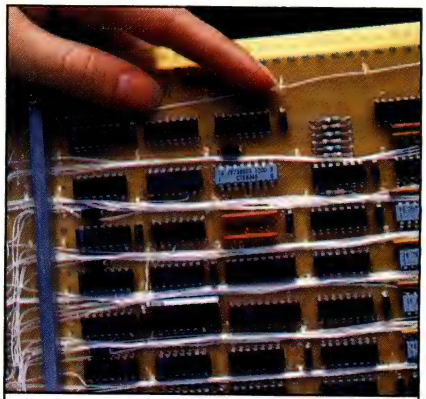
As a result, new laser diodes guarantee 5mW minimum output up to 60°C. They eliminate the need for thermo electric coolers and thus permit more compact equipment design. They also feature low threshold and operating currents: 20mA/50mA(25°C, 8mW).

The improved service life results in an estimated MTTF of more than 100,000 hours for 5mW operation at 50°C. Other features include stable fundamental transverse mode and nearly circular beam.

NEC
NEC Corporation
Tokyo, Japan.

A Texas Control

Months ahead of the market, Control Data is delivering the DDC (Director-to-Device Controller) interface on its 33800 Disk Storage Subsystem. It's an extremely compact, high-speed, large-capacity unit. Most important, it is the only available mass-storage subsystem plug compatible with the new-generation IBM DDC. What helps give Control Data this competitive edge? The SN75174 line driver from Texas Instruments.



Only TI's SN75174 line driver could provide the drive capability vital to Control Data's new 33800 disk storage subsystem featuring DDC interface.

No choice but TI

Only TI's SN75174 could provide sufficient differential current drive through Control Data's special compensation circuit to deliver proper signals in the DDC interface cable.

And Control Data will be able to stay current with future market developments because of the minimum active-high drive (40 mA) capability of the '174.

Forty-two '174s are used in a fully configured 33800 disk storage subsystem.

TI's SN75126 and SN75127 are also used in the new storage subsystem. These circuits meet the IBM 360/370 specifi-

◀ **Leading the market,** Control Data is shipping the first non-IBM storage subsystem that's plug compatible with the IBM Director-to-Device Controller interface. Use of TI's new SN75174 line driver not only made the Control Data design feasible but also minimized design time, component count, board size, and power requirements.

27-4812

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Instruments line driver drives Data to market faster.

cation, providing fault protection and power up/power down protection, as well as enable and fault flags.

Performance as specified

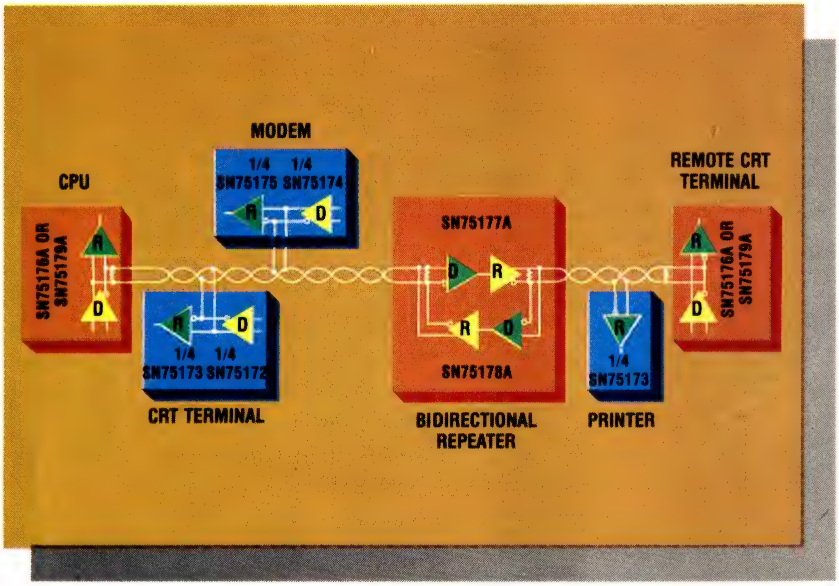
Control Data engineers learned about the '174 early on. Moving quickly, they evaluated and designed it in, counting on it to perform to very exacting specifications. It did . . . perfectly.

The alternative? Greater costs

Control Data engineers estimate that a discrete-component alternative would have resulted in at least a 15% increase in board area to accommodate the necessary additional components.

As it turned out, the SN75174 driver contributed important system savings to the design, improved reliability, helped Control Data get to market faster. ■

Get on the party line faster with eight new line circuits from Texas Instruments.



Hooking 32 driver-receiver pairs on a single bus to achieve party-line communication is possible with TI's full family of line circuits.

Now, eight new line drivers, receivers, and transceivers from Texas Instruments allow you to implement party-line applications on a single bus efficiently.

SN75176A
Half-duplex Transceiver

This new circuit wraps the capability to send or receive data over a single twisted pair in a compact, 8-pin package. It saves board space and cuts component cost.

SN75179A
Full-duplex Transceiver

Also available in a space-saving, 8-pin package, the SN75179A can send and receive data simultaneously, and requires two twisted pairs.

SN75177A/SN75178A
Bus Repeaters

These two differential ICs are identical except for complementary enable inputs. The SN75177A is active high and the SN75178A is active low. This allows you to pair the two back-to-back for improved bidirectional communication when extending cable distance.

SN75172/SN75174
Quad Drivers,
SN75173/SN75175
Quad Receivers

The two quad drivers operate from a single +5 V supply, yet maintain a high-impedance output over a common-mode range from −7 V to +12 V with power on or off. Without sacrificing speed. Both drivers have maximum delay times of 50 ns, rise and fall times of less than 80 ns. They allow data rates up to four megabaud.

The major difference between the two drivers is the enable scheme. And this increases design flexibility. All four drivers in the SN75172 are enabled at once, whereas they are enabled in pairs in the SN75174.

The two quad receivers are similar to existing RS-422 devices but have higher input impedance and extended common-mode range, from ±7 V to ± 12 V. Sensitivity is ±200 mV over −12 V to +12 V common-mode range.

All other standards covered, too

In addition to offering these new devices that meet RS-422 and other party-line applications, TI offers the industry-standard ICs you need to meet the EIA RS-485, RS-232-C, and RS-423 standards, as well as IEEE 488.

In fact, with its wide selection of general-purpose line circuits, TI fields the industry's broadest line of line circuits. Results: Component compatibility, design flexibility, and immediate availability.

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News update

A year after its introduction, the Zeropower random-access memory with piggyback batteries from Mostek Corp. [*Electronics,* May 5, 1983, p. 47] is surpassing the sales expectations of company officials. Moreover, the Carrollton, Texas, company has been swamped with inquiries from other memory-chip makers who want to provide a much needed second source.

The United Technologies Corp. subsidiary is now planning a significant cost reduction on the 2-K-by-8-bit nonvolatile static RAM. By early 1985, prices for the MK48Z02 are expected to fall from $22 to the low teens in 1,000-piece quantities. Also, a 64-K Zeropower chip—the 8-K-by-8-bit MK48Z08—is now in the works.

In the memory marketplace, the complementary-MOS Zeropower RAM is competing head-on with other new read-write nonvolatile semiconductor technologies—in particular, with electrically erasable programmable read-only memories and with shadow RAMs, which team conventional random-access memory cells with on-chip EE-PROM.

Buttons and hats. The Zeropower RAM derives its nonvolatility from two lithium battery buttons lying side by side in a plastic "top hat" that is then attached to a dual in-line package holding the die. Mostek's tests indicate that battery-backed data will be held in the RAM's cells for about 10 years.

To cut production costs, the firm is planning to use a new C-MOS process that will cut geometries from 3 micrometers to 2 μm and the die size from 65,000 square mils to 35,000 mils^2. It will also switch from its original configuration to a lower-cost top-hat assembly, which has fewer pieces to assemble and is more suitable for the greater automation of production lines.

As for 48Z02 chips that do not measure up to the Zeropower's low-current drain specifications of 600 nanoamperes at 80°C, Mostek is packaging them in standard 24-pin DIPs without batteries and selling them as 2-K-by-8-bit MK6116 static RAMs. **–J. Robert Lineback**

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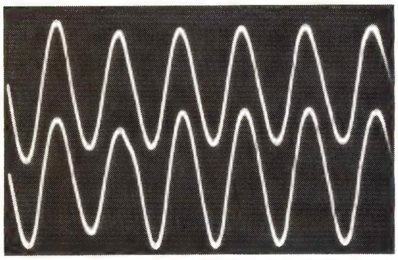

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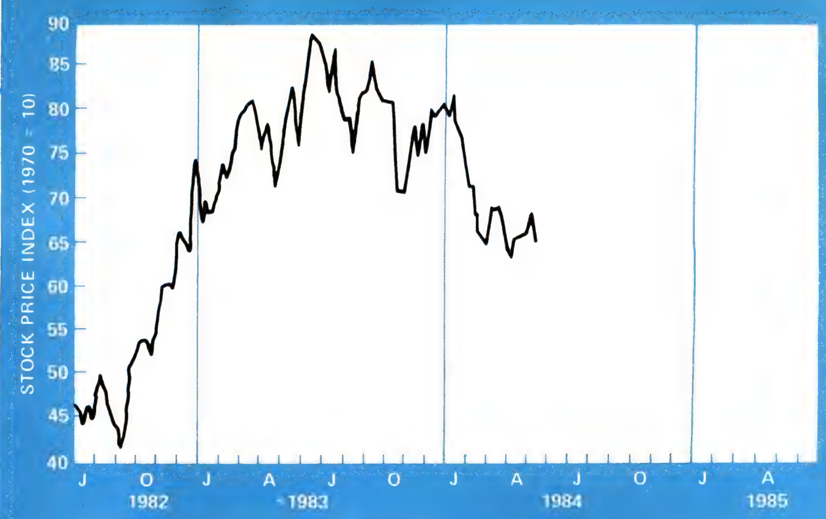
Business activity

"Trends in instrumentation stocks" records the stock market activity of a selected group of publicly owned manufacturers of test, measurement, and analytical instrumentation. The index weights the companies by size and therefore reflects their relative performances.



TRENDS IN INSTRUMENTATION STOCKS

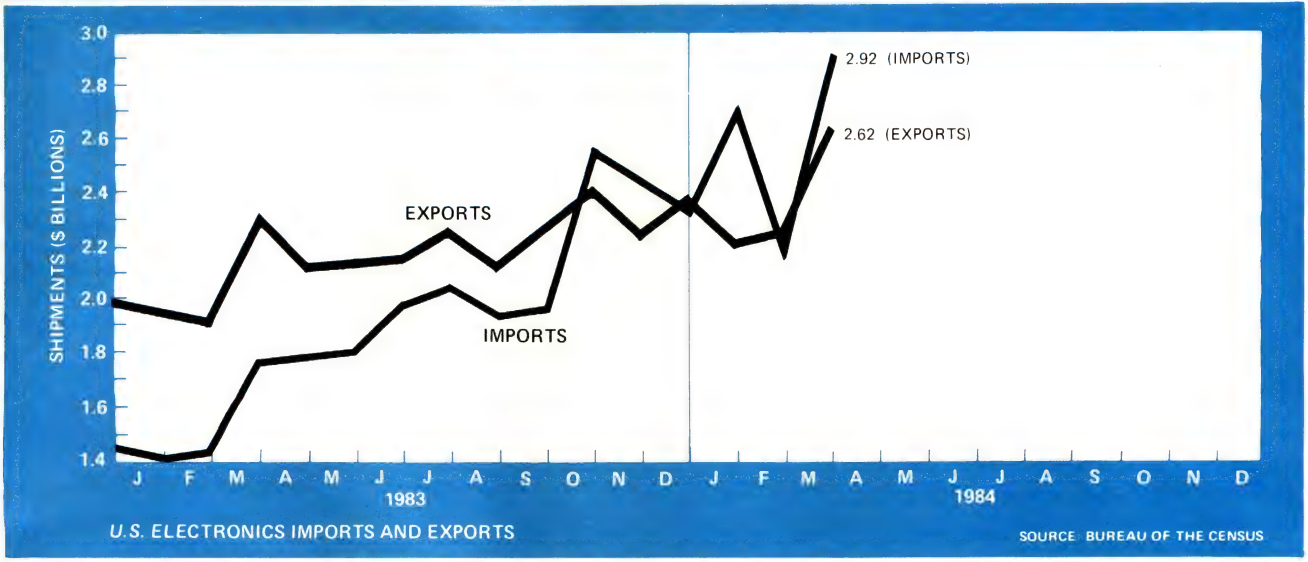
SOURCE: STANDARD & POOR'S CORP.

Predictions of higher interest rates in U. S. financial markets in the months to come do not bode well for companies that do business overseas—including electronics firms. High interest rates in the U. S. usually mean that the dollar stays strong overseas, and the chief economist of international consulting firm Arthur D. Little Inc., Cambridge, Mass., sees this trend continuing throughout the year. A. George Gols predicts that the strength of the dollar, which is high versus most of the major currencies of Europe, will decline by no more than 5% during the next six months. As long as interest rates in the U. S. remain high compared with those of other countries—especially America's major trading partners—the demand for and the value of the dollar will stay high. However, according to Gols, a sharp drop in U. S. interest rates might not cause the value of the dollar to fall overseas, since such a move would probably be accompanied by a proportionate decline in interest rates in Europe and Japan. Besides high interest rates, other factors working to keep the dollar strong include the lead by the U. S. in the world economic recovery, stronger long-term growth prospects, and political stability.

"While a strong dollar may be good news for international travelers, it has a negative effect on the earnings of U. S. companies with high stakes in foreign operations or exports, as well as those in competition with imports," says Gols. He expects pressure on foreign earnings to be most severe on companies that derive up to 30% of their profits from overseas operations. "Hedging can be costly and perhaps impossible in the case of restrictions on repatriation of earnings by less-developed countries," the economist notes. U. S.-based firms should use such techniques as intracompany trading and borrowing to minimize the effect of currency fluctuations, he advises.

Company financings . . . *Sequent Computer Systems*' second round of financing brought the Portland, Ore., firm $7.5 million. It plans to build a family of computer systems running under AT&T Bell Laboratories Unix operating system. . . . Integrated-software-systems supplier *Systems Center*, Irving, Texas, raised $3 million in its second round of financing. . . . A first round of financing provided *Vitelic Corp.*, Santa Clara, Calif., with $7 million. The company is planning to make complementary-MOS very large-scale integrated memories. . . . Semiconductor-pressure-sensor maker *Sensysm Inc.*, Sunnyvale, Calif., successfully completed a $1.5 million second round of venture financing. **–Robert J. Kozma**

Business activity



U.S. ELECTRONICS IMPORTS AND EXPORTS

SOURCE: BUREAU OF THE CENSUS

U.S. ELECTRONICS IMPORTS AND EXPORTS[1] (MILLIONS OF DOLLARS)

	IMPORTS			EXPORTS		
	Mar. 1984	Feb. 1984	Mar. 1983	Mar. 1984	Feb. 1984	Mar. 1983
Accounting, computing, and data-processing machines	281.551	208.577	125.474	596.159	492.703	490.650
Calculators	50.282	32.141	33.028	7.305	7.555	8.653
Parts for data-processing machines and office calculators	371.768	268.404	197.672	535.475	489.063	440.751
Telecommunications, sound-recording, and sound-reproducing equipment	1,226.447	1,023.293	813.349	362.427	287.958	357.322
Electronic or electric instruments	128.755	90.711	82.974	573.726	464.978	524.454
Printed-circuit boards	16.523	15.666	21.339	22.615	18.390	15.249
Integrated circuits, diodes and other semiconductors, tubes, piezoelectric crystals, parts	816.055	483.509	473.475	502.367	458.817	382.122
Fixed and variable resistors	25.738	22.542	14.649	15.804	14.639	11.271

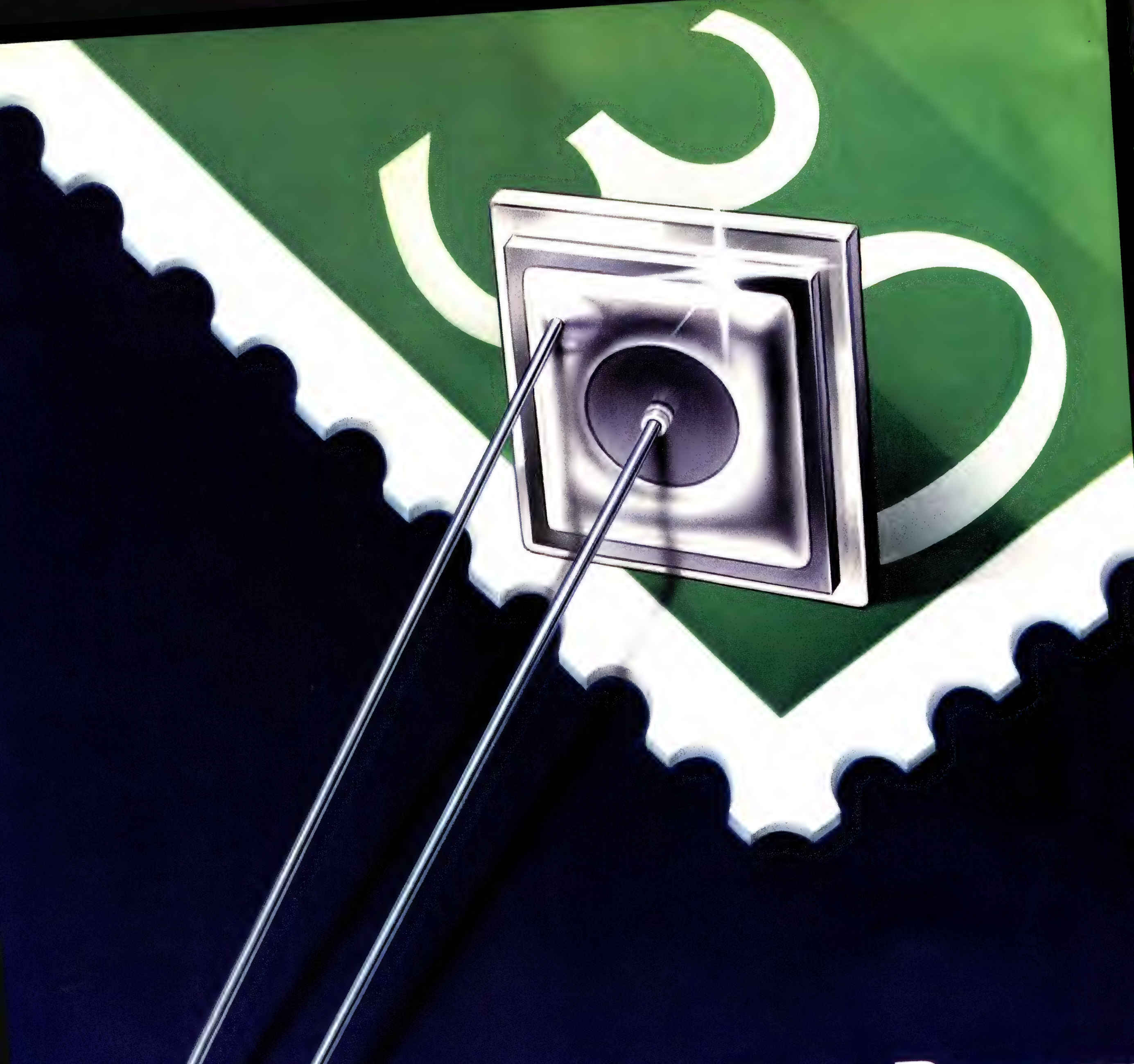
U. S. ELECTRONIC-COMPONENTS PRODUCER PRICE INDEX[2] (1967 = 100)

	April 1984	March 1984	April 1983
Digital bipolar integrated circuits	63.2	63.1	60.5
Digital MOS ICs	44.0	45.4	40.6
Linear ICs	64.2	63.5	60.8
Capacitors	191.8	192.2	190.0
Resistors	182.9	187.3	183.5
Relays	303.0	303.0	232.0
Connectors	226.9	225.8	220.6

GENERAL U. S. ECONOMIC INDICATORS

	April 1984	March 1984	April 1983
Average prime rate (%)[3]	11.93	11.21	10.50
Retail sales ($ billions)[4]	103.400 (March '84)	105.744 (Feb. '84)	93.804 (March '83)
Unemployment rate (%)[2]	7.7	7.7	10.1

SOURCES: [1] Bureau of the Census [2] Bureau of Labor Statistics [3] Federal Reserve Board [4] U. S. Department of Commerce



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Tag's "S" series Subminiature Thyristors are chips mounted on a solderable substrate with pigtail leads. Tag's "M" series Microminiature Thyristors are solder coated chips with preformed radial leads. These devices allow designers to rapidly develop hybrid power circuits and eliminate critical chip interconnects.

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A Raytheon Company

Circle 37 on reader service ca

The importance of getting the most out of the investments you make.

This man isn't getting the most from his umbrella investment. GenRad believes many electronics manufacturers aren't getting the most from their ATE investment. We can show you how your ATE can dramatically improve the quality of your products.

Many times, companies faced with problems have the solutions to those problems close at hand.

This can be especially true for many electronics manufacturers.

These companies are faced with the problem of improving the quality of their products. And improving productivity and profitability.

And like the man above, these companies have the solutions to their problem close at hand.

The solution is their automatic test equipment (ATE) and how they make the best use of it.

GenRad can show you how to solve the problem of improving the quality of your products. By showing you how to get the most from your ATE investment.

We call this concept Quality Management.

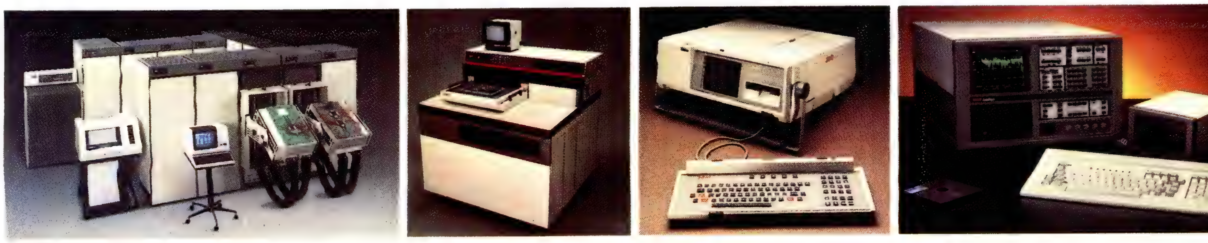
Why ATE is such an important investment.

Chances are, you're already using ATE.

To test components, subassemblies and finished assemblies.

Your ATE helps you find out what's good and what's bad. If it's bad, you weed it out or repair it.

But this method is simply *measuring*



GenRad offers the broadest line of testers in the industry. We offer systems spanning the total Engineering/Manufacturing/Service process.

quality. Finding defects after they've already occurred.

Today, measuring quality isn't enough. You must learn to *manage* quality.

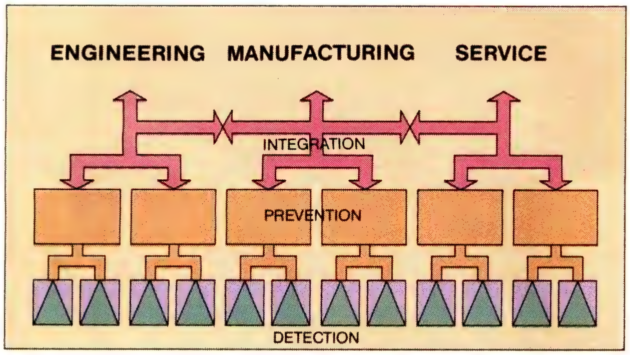
When you manage quality, you can improve the *process* that creates your products.

You can *prevent* faults instead of just finding them.

But first, you must learn how to leverage your ATE investment.

How to leverage your ATE investment.

Any systematic approach to Quality Management must start with the data created by ATE.



There are three levels of Quality Management. Level 1 is fault detection. Level 2 is fault prevention. Level 3 is the integration of quality information throughout the entire process. As you can see, Quality Management builds up from a solid base of testing capability.

There's simply no place else to get it.

But that data by itself won't help you improve quality. Unless you *leverage* it.

To leverage, you must apply powerful Quality Management Software to sort reams and reams of test data. And extract meaningful quality information.

Then you must put that quality information to use where it can do you the most good.

When you leverage, you'll be able to identify trends. You'll be alerted to emergency situations. And you'll be able to monitor the extent of improvements in quality. Automatically and in real-time.

As a result, you'll be able to actually manage and improve quality. And you'll get a better return on your ATE investment.

The solution is at hand today.

Quality Management is not some futuristic notion.

But to make Quality Management work, you do need three things.

First, you need ATE. And GenRad offers the broadest line of ATE in the industry.

Secondly, you need to learn to leverage. Again, GenRad offers the tools you need, hardware and software, that can help you move to higher levels of quality.

Already, several of our Quality Management products are helping customers realize significant improvements in quality.

Products like TRACS™ – a system that helps you lower costs, reduce in-process inventories, and dramatically increase the capacity of your production test and repair process.

And SCAN™ – a system that helps you improve the quality of incoming components and the productivity of your incoming inspection process.

Finally, you need a company that's willing to work with you in solving your special problems. GenRad provides more of that kind of custom applications support than anyone in the industry.

GenRad's approach to Quality Management.

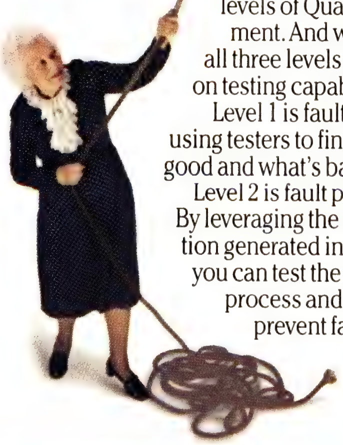
At GenRad, we believe there are three levels of Quality Management. And we believe all three levels depend on testing capability.

Level 1 is fault detection – using testers to find out what's good and what's bad.

Level 2 is fault prevention. By leveraging the information generated in Level 1, you can test the entire process and fix it. You prevent faults instead of just finding them.

Level 3 is the integration of Quality Management – where quality information is disseminated throughout the engineering, manufacturing and service process, and up to your broader purpose business control system.

GenRad offers products at all 3 levels.



When you use leverage, you can perform tasks that would be otherwise impossible. GenRad can show you how leveraging your ATE investment can dramatically improve quality.

Quality Management of Board Testing
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GenRad's Approach to Quality Management
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"I'm tired of talking about quality. I need to manage it."

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And sealed construction eliminates both maintenance and leakage problems.

There's also the versatility. Our cells can be assembled into an endless variety of configurations. They are rated at 2 volts with capacities of 2.5 Ah, 5 Ah, 12.5 Ah and 25 Ah.

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Electronics newsletter

Epitaxial wafers gaining favor as C-MOS base

Even though they cost two to three times more than ordinary silicon, epitaxial wafers are becoming the starter material of choice for making complementary-MOS chips. An epitaxial layer, with a different resistivity than its substrate, eliminates latchup in C-MOS without space-consuming corrective techniques, and IC makers are finding that increased yield more than makes up for the extra expense. **Monsanto Electronic Materials Co., Palo Alto, Calif., this month became the latest manufacturer to make a significant production commitment.** Others already in the field are SEH America and Cincinnati Milacron, and at least half a dozen wafer companies were advertising epitaxial wafers at last week's Semicon show in San Mateo, Calif. Despite the promises, however, supplies depend on the availability of epitaxial reactors, for which makers are quoting 10-month delivery times.

Laser printer joins HP line of personal computers . . .

Completing its promised four-phase entry into the personal-computer market, Hewlett-Packard Corp., of Palo Alto, Calif., introduced at Comdex, in Atlanta last week, a laser printer. Called the LaserJet, the $3,495 printer **uses the same disposable print cartridge and paper-handling system as Canon's LBP-CX laser printer**. It follows the HP 150 personal computer, the ThinkJet printer, and the Portable to the market. The LaserJet will work with other personal computers, such as the IBM PC and its compatibles, and with software packages like Lotus 1-2-3, Multimate, WordStar, and PFSWrite.

. . . as firm claims No.3 spot in market

Hewlett-Packard also said at Comdex that research it commissioned shows it has eclipsed Tandy Corp.'s Radio Shack for third position in the personal-computer market. According to the research, **the 1984 market will be about $12 billion,** with IBM taking 30.3%, Apple 20.7%, HP 6.1%, and Tandy 5.2%.

$495 card for PCjr puts it on Omninet

Independent makers of peripherals are beginning to go to market with enhancements for IBM Corp.'s PCjr, the home computer whose sales thus far have been disappointing. For example, in July, Corvus will introduce a networking capability **that should make the computer more alluring, especially to the educational market,** a segment in which the machine has had little success. The San Jose, Calif., company's $495 transporter card will allow the PCjr to operate as a node on Omninet. Similarly, a Utah firm has brought out a kit containing added memory and other features (see p. 121).

Calma will expand CAE layout to boards

Calma Co., the Santa Clara, Calif., subsidiary of General Electric Co. that pioneered automation of chip layouts in the 1970s, is about to demonstrate a renewed thrust in electronics-engineering markets with a system that marries computer-aided engineering and printed-circuit-board design. It will be unveiled at Cadcon-East, in Boston, June 11. **Dubbed T-Boards, the package ties logic-schematic capture and pc-board layout with a common data base in TegaStation,** a CAE environment for Apollo work stations from Calma's new branch in Austin, Texas. T-

Boards, which can do 32-by-32-in. 16-layer boards, features pop-up menus, automatic interactive routing with up to eight layers done simultaneously, real-time checks to ensure that a layout implements design, and 1-mil precision. Including a DN660 Apollo computer with 160-megabyte disk, T-Boards will cost $100,000, with deliveries expected in the fourth quarter. With the TegaStation environment, T-Board users will also be able to tap into Calma's semicustom gate-array package—called T-Arrays—slated for introduction later in June at the Design Automation Conference in Albuquerque, N. M.

ICL and AT&T team on value-added net

Britain's ICL plc will use equipment supplied by AT&T International, the overseas marketing unit of AT&T Co. , in a value-added network the British company is planning to operate. The market, still in its infancy in the UK, is growing at 20% to 25% a year and will be worth up to $1.32 billion by the late 1980s, according to ICL. **Deregulation of British Telecom has opened the way to private companies to compete in this sector.** AT&T already operates such a network—NET 1000—in the U. S.; it will supply Britain's flagship computer company with packet switches, protocol processors, and an international gateway linking the two companies' networks. Both are based on the International Organization for Standardization's reference model for open-systems interconnection. ICL will be challenging IBM Corp., whose first value-added network in the UK is likely to be a joint effort with British Telecom to provide an electronic funds-transfer system.

Addenda

National Semiconductor Corp., of Sunnyvale, Calif., says that the Academic Information Systems Business Unit of IBM Corp. **will purchase a version of National's Genix 32 operating system,** which is based on Berkeley 4.2 BSD Unix. The Stamford, Conn., IBM unit will use Genix experimentally in several university projects that it refuses to identify further. . . . Following joint-manufacturing and -marketing announcements that make it the **first major U. S. retailer to enter the cellular mobile-telephone business,** Tandy Corp., of Fort Worth, Texas, promises to more than double its number of U. S. specialized phone centers, from 25 to 55. "We are a serious long-term player in the telecommunications marketplace," vows John V. Roach, president and chairman of Tandy, which earlier in May announced it would jointly design and make cellular phones with Mobira, a subsidiary of Oy Nokia, in Helsinki, Finland. . . . Another vote for the 3.5-in. form factor in microcomputer memory peripherals (see p. 45) was cast at last week's Comdex by a start-up from Milpitas, Calif., called InterDyne Co. Its disk drive, **intended for streaming backup of hard-disk drives,** fits in a hole that measures 1.62 by 4.00 by 6.00 in. . . . The new trustees of the Howard Hughes Medical Institute, owner of Hughes Aircraft Co., were scheduled to meet May 29. **Expected to be on their agenda was the sale of the El Segundo, Calif., aerospace company,** an effort that has been stalled by litigation. . . . Considered a precedent-setting pact involving the Government's new weapons-warranty program, **the U. S. Navy has awarded $401.6 million to Texas Instruments Inc.** for production of 798 high-speed antiradiation missiles (HARM). There is an option for an additional 1,320 missiles at a maximum of $492.8 million.

Memory makers ponder wordwide megabit chips

by J. Robert Lineback, Dallas bureau

Mostek pushing by-16-bit layout in 28-pin package as Jedec unit weighs pinout standards and manufacturers consider options

In memory-chip circles, the latest word is 16 bits wide and housed in a 28-pin package with multiplexed address and data bits. That is what Mostek Corp. is advocating after announcing a 16-bit-wordwide memory concept for parts that store a megabit or more.

The move—which surprised an industry committee studying pinout proposals—may signal the start of a major pinout skirmish as chip merchants attempt to set standards for the next generation. Some, however, believe that the coming megabit-memory markets, unlike the current ones, may be large enough to support multiple pinout standards.

By multiplexing address and data signals on the same pins, Mostek says, the industry can avoid larger 40-pin dual in-line packages while housing up to 8 megabits of read-only memory and 4 megabits of writable memory in 28-pin DIPs. In the fourth quarter, the Carrollton, Texas, subsidiary of United Technologies Corp. plans to introduce its first wordwide chip: a complementary-MOS megabit ROM (64-K by 16 bits), dubbed the MK3901.

For now, Mostek is campaigning to make the 28-pin footprint an industry pinout standard for future random-access memories, ROMs, and other nonvolatile chips, such as electrically erasable programmable ROMs. At issue is the best memory package and configuration to serve emerging microprocessor-based systems with data buses that are 16 bits wide. To date, 16-bit systems had to rely on memory chips that present data 8 bits at a time, more suitable for bytewide (8-bit) data buses than for wordwide ones, says Howard Sussman, application engineering manager at Mostek.

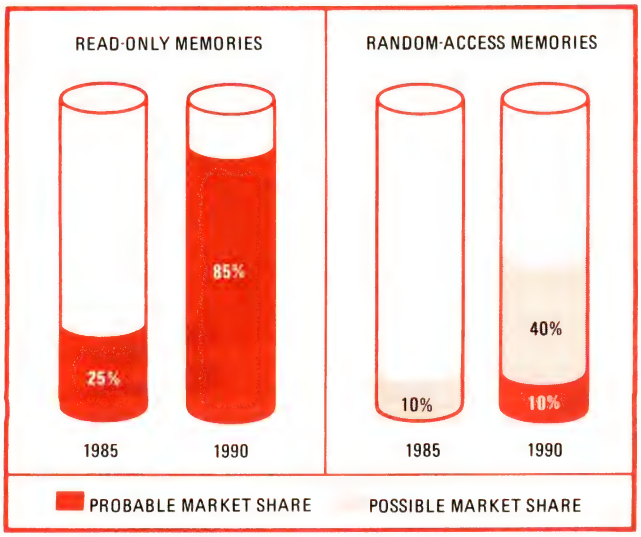
In the late 1970s, Mostek established the ByteWyde memory concept, a compatible 28-pin footprint for by-8-bit memories. Now an industry standard, the by-8-bit format runs out of pins at a megabit.

For some customers, a 40-pin nonmultiplexed ROM or EE-PROM may be easier to accept than the added logic and design work it will take to interface multiplexed memories with some popular 16- and 32-bit processors, cautions Ken Kwong, who is director of product marketing at Seeq Technology Corp., the San Jose, Calif., EE-PROM firm. Many processors have separate pins for address and data bits. Kwong believes the industry will support both 40 and 28 pins.

A surprise. Both schemes are being considered by the Joint Electron Device Engineering Council's 43.2 memory committee. Formally proposed last year, Mostek's wordwide pinout was reportedly stalled in the negotiation process. Not wanting to delay its megabit 3901 ROM, Mostek elected to make its wordwide campaign public just days before this month's Jedec 43.2 meeting, catching many members off guard.

Mostek's proposal is designed to operate in either 8-bit-byte or 16-bit-word modes. In addition to fitting into the 28-pin DIP, the Mostek pinout organization is suitable for square 32-pad leadless and leaded chip-carriers, says Sussman.

Interfaces to some 16-bit microprocessors, such as Intel Corp.'s 8086 line and its 186, can be direct since address and data are multiplexed on these processors, he notes. For other nonmultiplexed processors—such as Motorola Inc.'s 68000 and Intel's new 286—only two extra logic chips are



Looking ahead. Mostek projects consumption of megabit wordwide ROMs and dynamic RAMs to grow quickly to 1990. However, the question is how fast—particularly since RAMs will tend to be used in small systems needing a single chip—hence the wide swing for 1990.

needed to demultiplex the memory's address-data signals. Mostek is already working with customers on such a design.

Jury still out. However, other memory makers are still undecided on megabit pinouts. Intel, in Santa Clara, Calif., is expected to make its decision known by fall. Texas Instruments Inc., of Dallas, and Motorola's MOS memories operation in Austin, Texas, are still thinking.

The Japanese are reluctant to talk about plans for by-16-bit memories. Some parts have surfaced, however. Oki Electric Industry Co. is selling at home a wordwide megabit ROM as a character generator, and NEC Corp. has announced an E-PROM. Mitsubishi Electric Corp. says it has no plans for the memories because it is mostly concentrating on large-system applications.

Inmos Corp., of Colorado Springs, Colo., believes address-only multiplexing should be used to keep high-density memories in 28-pin packages, but prefers bytewide configurations for higher performance, says Ron Sarbre, senior applications engineer. Inmos says it will back a standard.

However, the head of Jedec's committee 42.3 does not expect an approved wordwide pinout standard in 1984 and says there is still time for more input, "especially from the chip users because that is what standards are ultimately for," adds David C. Ford, who expects wordwide standards in 1985.

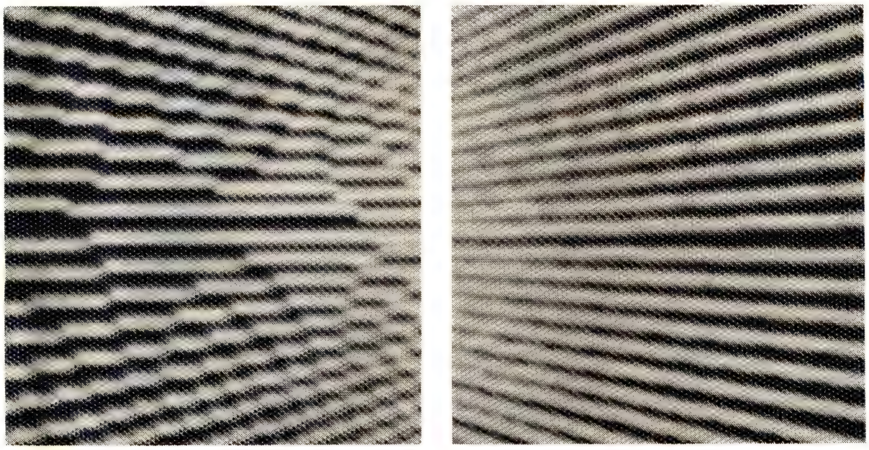
Graphics

Advanced multifunction computer systems leave stand-alone graphics terminals in dust

For suppliers of computer-graphics gear, the fail-safe route to growth has been the well-trodden path of equipment improvement: better application packages along with ever-higher-resolution displays—both taking advantage of speedy new microprocessors and cheaper memory. The payoff is a business now running at a $4.5 billion annual rate and still expanding at a 30% yearly clip.

But it appears that such a game plan no longer will suffice. That is the message accompanying a new kind of graphics system—one that is actually more powerful than general-purpose computing equipment containing advanced graphics. The new systems received much attention earlier this month in Anaheim, Calif., at Computer Graphics 84.

Unix popular. For openers, the new equipment provides standard operating systems (mostly with AT&T Bell Laboratories' Unix as a base), an integrated data base for manipulating nongraphical business and scientific information, along with communications functions for networking and linking up with external data sources. Soon to come are better multifunction software programs to link different tasks, as well as general-purpose analysis packages.



Getting it *straight*. New graphics terminals are actually computers with special features. For example, the Megatek 9200 reduces staircases (left) found in traditional raster displays.

Although the trend has accelerated so quickly that even some industry veterans have been surprised, its impetus is unmistakable. Predicts Johan Brag, chairman of Brag Systems Inc., a San Mateo, Calif., software supplier, "There's really not much future for the stand-alone graphics terminal. Users want their hardware tied into multifunction software," and suppliers will provide it, or risk missing out.

Brag goes even further when he says, "Computer graphics will disappear as a separate industry. To reap the benefits, suppliers will have to offer more."

By most accounts, Silicon Graphics Inc., of Mountain View, Calif., started the trend in late 1983, when it introduced IRIS (Integrated Raster Imaging System) [*Electronics,* Oct. 20, 1983., p. 113]. Crucial is a key development supporting the multifunction machines: very-large-scale integrated circuits that expand performance.

Competitors are now rushing their entries to market. For example, Megatek Corp., of San Diego, Calif., has its Merlin 9200, an advanced unit that incorporates a hierarchical data base, multiprocessor computing, and networking. For three-dimensional graphics tasks, it operates as fast as 100,000 16-bit vectors per second. It sells for about $45,000, including options.

For business. Lexidata Corp., of Billerica, Mass., has a new family, LEX 90, that it touts as more than a graphics system meeting new technology requirements. "It is specifically designed to be as appropriate from a business standpoint," says Jack Huisman, product marketing manager. Its hardware and software are modular, so it can be upgraded; base prices are in the $20,000 range.

From Ramtek Corp., in Santa Clara, Calif., comes a pair of end-user models that merge geometry processing and display generation into a general-purpose environment. Models 7115 and 7215 sell for $28,000 and $44,000, respectively. And there are others, among them Saber Technology Corp.'s Interactive Graphics Computer System [*Electronics,* May 3, p. 183] and Cal-Comp's system 25 (see p. 114).

Because the new equipment is still in its infancy, some firms may not have come to grips with all the changes it forces. For one, selling what amounts to a full-fledged minicomputer raises the equipment-support level. Also, the advent of systems with software-intensive general-computer capacity will speed up the shakeout in the business, maintains James H. Clark, founder and chief technical officer of Silicon Graphics.

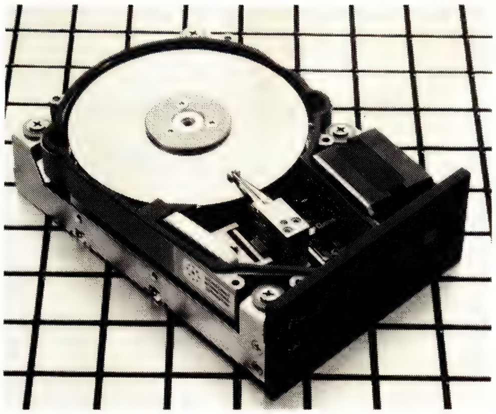
"Companies only doing peripherals will find it tougher to make the transition," he says. Computer companies selling into the graphics business could also feel the heat, in Clark's view. **–Larry Waller**

Memories

Micro-Winchesters lure more makers

For more than a year, SyQuest Technology, of Fremont, Calif., and Rodime plc, of Glenrothes, Scotland, have had the micro-Winchester disk-drive field pretty much to themselves as most drive makers concentrated on exploiting mass and high-end markets for 5.25-inch models. But now the size, weight, and power advantages of even smaller equipment are luring other firms into the field, and as many as half a dozen sub-5.25-in. drives may be on the market by the time of the National Computer Conference, in July.

All the new drives are based on the 3.5-in. disks in half-height packages that match the form factor developed by the Sony Corp. for its 3.5-in. microfloppy drive. SyQuest continues to favor the 3.9-in. size it introduced two years ago in a combination of fixed and removable cassettes (and has now augmented with three fixed-only drives); but even Syquest is looking at the half-height 3.5-in. form.



Small package. Microscience International is one of the newcomers offering a 3.5-inch *half-height* microfloppy Winchester disk drive, which carries a $400 price tag.

The newcomers include Microscience International Corp., of Mountain View, Calif.; LaPine Technology Corp., of nearby Santa Clara; and Microcomputer Memories Inc., of Van Nuys, Calif. All three will offer 5 and 10 megabytes of formatted storage in 3.5-in. half-height drives: 1.625 by 4.0 by 5.75 in. They not only fit in the same slot as a Sony microfloppy but also fit sideways into a 5.25-in. slot.

"I would expect to see announcements from several others," says analyst Jim Moore, of Dataquest, a San Jose, Calif., market-research firm. "The initial installation path will be in transportable and portable computer systems, the same market as for the half-height 5.25-in. drives."

Besides the announced starters, three others—Seagate Technology, of Scotts Valley, Calif.; Tandon Corp., of Chatsworth, Calif.; and Miniscribe Corp., of Longmont, Colo.—are also said to be working on 3.5 inchers.

Control Data Corp., Minneapolis, introduced a 3.5-in. unit called the Cricket last year, but withdrew it because it considered the capacity (6 megabytes unformatted) too low. It is reevaluating its product, but has not scheduled reintroduction.

"The big-volume players are in no rush to announce because of the large volumes in their current product lines," Moore says. "Entries by smaller companies may force them into production, however." Rodime has announced a $50 million order with Televideo Systems Inc. and is also selling its half-height drives to Compaq Computer Corp.

Another analyst, James Porter of Disk/Trend, Mountain View, Calif., has estimated that by 1986, half of the annual consumption of all drives with under 30 megabytes of storage, about 4.7 million units total, will be 3.5-in. units. Initially, the micro-Winchesters may cost a little more than their 5.25-in. counterparts, but they will weigh a third as much and consume half the power.

Microscience, whose drive includes three proprietary large-scale integrated circuits, plated media and Whitney heads, and a closed-loop servo, projects a price of $400 in large quantities. LaPine, in addition, promises a shock-resistant design in which the heads can be moved away from the disk when the equipment is being transported. **–Clifford Barney**

Trade

Dollar-yen deal called breakthrough

In a major move termed "long overdue" and "extremely significant" by the Semiconductor Industry Association, the U. S. and Japan will shortly seal an agreement aimed at lowering the value of the yen in relation to the dollar. U. S. trade officials believe it will increase Japan's demand for U. S. goods while slowing down its export drive.

"We expect this to greatly facilitate current efforts by U. S. semiconductor makers to step up sales to Japan," says Warren Davis, a spokesman for the trade group, which has its headquarters in San Jose, Calif. "In the long run, the restructuring of Japanese currency markets could prove to be the most important measure for redressing the bilateral trade imbalance," he adds.

The agreement, expected to be announced at the early June summit of Western heads of state, is designed to promote internationalization of both Japan's currency and capital markets. For example, Tokyo is likely to approve the issuing of yen-denominated bonds and securities abroad and to loosen restrictions on U. S. deposits and borrowing. This would increase demand for the yen, thereby causing it to appreciate.

The hope is for the yen to drift closer to an exchange rate of 200 to the dollar, versus about 233 today, thus improving the cost-competitiveness of U. S. high-tech products, says Davis. Direct U. S. investment in Japan should also increase markedly. Easier foreign access to Japanese financial markets on terms more in line with the practices of Western advanced industrialized nations should attract both U. S. banks and companies, he predicts.

But some business officials are less sanguine about the prognosis for more equitable trade. They question just how much Tokyo will subject its economy to international influences—especially if the consequences are negative, such as rising interest rates and loss of world-market share. Yet any step toward making Japan a full-fledged member of the world financial community is welcome.

"But don't expect a miracle overnight," warns Lawrence Fox, vice president for international affairs for the National Association of Manufacturers. As many economists point out, high U. S. interest rates and budget deficits are the main causes of an overvalued dollar. –**Karen Berney**

Materials

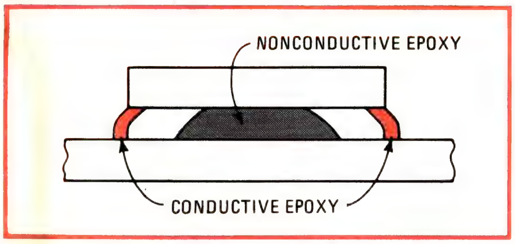
Epoxy called better than conventional solder for surface-mounting components on boards

For the fast-growing business of surface-mounting components, a Billerica, Mass., company has come up with a technique that promises more reliability, higher yields, and lower cost than the usual solder method. Epoxy Technology Inc. uses electrically conductive epoxies to attach component leads or pads to the copper conductors of printed-circuit boards.

Soldering is rife with drawbacks. It cracks and requires relatively complex processing. In addition, solder and package metals leach.

Cracking, the most serious problem, is caused by the mismatch in the thermal coefficient of expansion between the board and a ceramic leadless chip-carrier, which stresses the solder joint during temperature cycling. Designers are working with substrates whose thermal coefficients almost match that of an alumina package; but Kevlar, copper-Invar-copper, and similar materials cost more. Electrically conductive epoxy, not as rigid as solder, will tolerate the stresses of thermal cycling.

The firm is evaluating two conductive epoxy types, Epotek H70E and H20E, on epoxy-glass multilayer boards with untinned leaded packages and leadless chip-carriers. These will be tested for board flexure, impact, thermal cycling, and electrical and heat dissipation.



Fewer steps. Conductive and nonconductive epoxies can be used without the pretinning, prebaking, and flux-removal steps that are required by solder.

Ranking right behind solder's material weaknesses is the number of steps required to use it. Each additional process—pretinning of substrate metalization, chip-carrier metalization, prebaking, solvent removal (which must be done after solder screening and before solder reflow), and more—increases the risk of damage due to handling.

On the other hand, conductive epoxy needs no pretinning, prebaking, or flux removal. Instead, it is screen-printed onto substrate metalization to a thickness of 2 mils. Then, dots of nonconductive epoxy are dispensed for added mechanical integrity, and components are placed and cured at 150°C to 200°C. Though conductive epoxy costs three times as much as solder, it more than makes up for that expense by requiring cheaper production equipment and fewer processing steps.

As for leaching, the tin in the solder dissolves metalization on chip contacts, meaning a poor electrical connection or even nonsolderability during reworking. Epoxies simply do not support leaching, so they provide a reliable electrical joint.

Epoxy Technology is attempting to simplify the production of boards still further with a copperless pc board with all its printed wiring consisting of screened-on conductive epoxy. Feasibility prototypes using this construction were made as far back as 1968, but the need for plated through-holes, which are not cost-effective, put a damper on the project.

Today's surface-mounted boards, however, do not need through-holes. So the firm is building surface-mounted computer-circuitry prototypes based on integrated circuits in small-outline packages and passive chip components to be tested against an equivalent soldered pc board in a computer. –**Jerry Lyman**

Communications

Telenet to encrypt electronic mail

GTE Telenet Communications Corp., of Vienna, Va., has a new weapon to deploy against the growing number of computer trespassers: a software-encryption package called Phasor Code. For a bit less than $600, it gives users of GTE's Telemail service levels of security "never before achievable," promises the product's developer, James H. Finch.

Finch is president of International Phasor Telecom Ltd., a Vancouver, B. C., firm that recently signed a long-term agreement giving GTE Telenet the exlusive right to market the Phasor Code public-key technique to its electronic-mail users. Although public-key algorithms have been around for five years, Phasor Code is "the first commercial implementation," as Finch puts it. Encryption experts agree.

Unlike private-key systems, which use the same key to encrypt and decrypt messages, Phasor Code relies on two distinct keys, explains David Brown, a program analyst who is one of the Canadian company's 13 employees. The first key, the public one, is made available to all users and performs encryption. The second key unscrambles the message but can be triggered only by the intended receiver with a personal password.

By using a public key for scrambling, Phasor Code eliminates the need to deliver a new printed-circuit board to change private keys when users depart. That has been the major drawback of conventional hardware-driven systems, typically selling for $3,000.

Phasor Code also promotes higher levels of security and faster processing than private-key designs do, the company claims. Its closest rival, the National Bureau of Standards' Data Encryption Standard, produces a 56-bit key. The Phasor algorithm generates an encryption key of 1,300 bytes and a decryption key of 512 bytes but adds 256 bytes to each coded message; the Data Encryption Standard adds just 8.

In tests, Phasor Code has transformed encrypted data eight times more quickly than the Data Encryption Standard does, claims Brown. Nonetheless, Government cryptology specialist Dennis Branstad, of the NBS, is wary. "We would really like to see the evidence," he says. The agency is currently evaluating public-key algorithms to make electronic mail secure but is a few years away from developing a standard, he reports. Meanwhile, he says, a new NBS cryptology-management standard based on the Data Encryption Standard has been adopted by the U. S. banking community. Implemented in hardware, the standard sells for $395 and runs on IBM Corp. Personal Computers.

ITT Dialcom, a competitor of GTE Telenet, is "moving in the direction of a systemwide security solution," reports Paul Warren, a spokesman for the Silver Springs, Md., firm. Warren says Dialcom is talking to Phasor about modifying the software in its product and thereby providing network-access control. "For that, we need an encryption capability that resides in the host computer or in a separate facility and can be activated by dumb terminals," he notes.

Only intelligent terminals can now decrypt Phasor-coded messages, and

News briefs

Docutel/Olivetti unveils 4-lb computer, discloses more losses

Docutel/Olivetti Corp., the Dallas vendor of automatic teller machines and electronic typewriters, continues to operate in the loss column but has nevertheless jumped into the competitive briefcase-size computer market with a four-pound model that was introduced at last week's Comdex/Spring show, in Atlanta. The M10 unit retails for $799 with 8-K bytes of memory ($999 for 24-K bytes) and can be plugged into the firm's new PL10 portable microprinter-plotter, selling for $260. Before the unveiling, Docutel/Olivetti reported a loss for the quarter that ended March 31 of $8.3 million on $37 million in revenues. For the same period last year, the firm lost $1.3 million on sales of $51.8 million. Also at Comdex, Morrow Designs Inc., of Richmond, Calif., introduced its competing 9-lb entry.

AT&T to build new digital switch in Taiwan

The American Telephone & Telegraph Co. plans to begin production of its ESS-5 digital switching system in Taiwan in 1985, under an agreement with Taipei's Telecommunications Administration and the local Bank of Communications. The deal, which is expected to be signed in June, calls for AT&T to invest 70% of the $40 million required for the project, with the remainder to be financed by the other two parties.

GM seeks to purchase Perot's Electronic Data Systems

General Motors Corp., New York, says it has initiated preliminary talks with Electronic Data Systems Corp. that could lead to its acquisition of the Dallas computer service firm. The price tag is expected to top $2.5 billion. EDS, still under the control of its founder and chairman, H. Ross Perot, had revenues of $651.6 million last year and has recently been winning big government contracts to link different kinds of distributed-computing systems for the Navy and Army. In an unrelated move, EDS has sold Centurion Computer Corp., of Richardson, Texas, back to its founder three years after buying the minicomputer firm [*Electronics,* March 24, 1981, p. 48]. No price was disclosed.

Addenda

After a year of heavy losses in its Data Systems division, Raytheon Corp. has announced that it is getting out of the highly competitive market for word processors and work stations. . . . The Senate has passed the Semiconductor Chip Protection Act, which will provide copyright protection for semiconductor designs. A related bill, H. R. 5525, is in the House. . . . Thomas P. O'Mahony has been named to head the Air Force Electronic Systems division's new deputy command for intelligence, countermeasures, and support systems. The new organization manages acquisition of more than 40 systems deployed worldwide and has its headquarters at Hanscom Air Force Base, Mass.

they must run the MS-DOS or PC-DOS operating system. The company says it is working to make Phasor Code compatible with other operating systems, too. –**Karen Berney**

Computers

IBM's Expo aims to woo Europeans

International Business Machines Corp.'s domination of the European computer market has engendered hostility from domestic manufacturers and the European Community. Now, in an attempt to establish a European identity, IBM is going to the people with a circus-like traveling show that will cover 20 major cities in 14 nations over the next three years.

Called Expo, the show is designed to communicate with a public that is not made up of computer specialists. It is a display of state-of-the-art data-processing technology meant mostly for young people, says Kaspar Cassani, president of IBM (Europe).

But overlaying the festive air of Expo is the reality of IBM's European situation. It has 30% of the market, and its strength does not sit well with competitors or governments.

In March, for example, an effort was launched to block the Armonk, N. Y., firm from imposing its System Network Architecture as a de facto standard. Twelve European manufacturers of data-processing equipment agreed to produce equipment based on common protocols [*Electronics*, March 22, p. 63].

Then the Common Market's commission refused IBM's appeal for a negotiated settlement to a three-year-old case in which the U. S. company is accused of having abused its dominant market position by withholding information about its large- and medium-computer interfaces from its competitors. However, the commission now says that it is in the final stages of negotiations with IBM to end the inquiry. It is also debating the question of IBM's participation in Esprit, for European Strategic Program in Information Technologies, the Common Market's bid to catch up with the U. S. and Japan in computers and office automation.

Although these issues will be of small concern to most visitors to Expo, the show can do little harm in improving IBM's public image. In the long run, then, it might strengthen the firm's political position.

High-tech fun. Expo-goers will be treated to a tour of modern information-processing technology, all presented in a hands-on atmosphere where they can touch, operate, and learn about holograms, robots, image processing, speech recognition, lasers, and computer programming. Some 56 guides, recruited from French universities, are on hand to explain the exhibits. More substantial technical explanations are available from IBM staff members. The show will be in Paris until June 26, then begin its tour. –**Robert T. Gallagher**

Consumer

EIA panel working on standard interface bus for makers of home electronics products

In the consumer-electronics industry, with its scores of products, manufacturers, and interconnections, the task of establishing standards agreeable to everyone in the business would be enough to reduce a Solomon to tears. Now there is a glimmer of hope, as a committee of the Electronic Industries Association will be going to work on a standard for a home bus.

The proliferation of electronic products in the home has made compatibility an important issue. But in an industry with many manufacturers and often more than one way to solve a single technical problem, establishing uniform standards is particularly difficult: witness the controversy surrounding a-m stereophonic transmission and the four techniques seeking market acceptance.

However, Judson Hoffman, of the Matsushita Technical Center, in Secaucus, N. J., believes it can be done. He is chairman of the EIA's Home-Bus Standards Steering Committee. The group is operating under the auspices of the association's Engineering Policy Council.

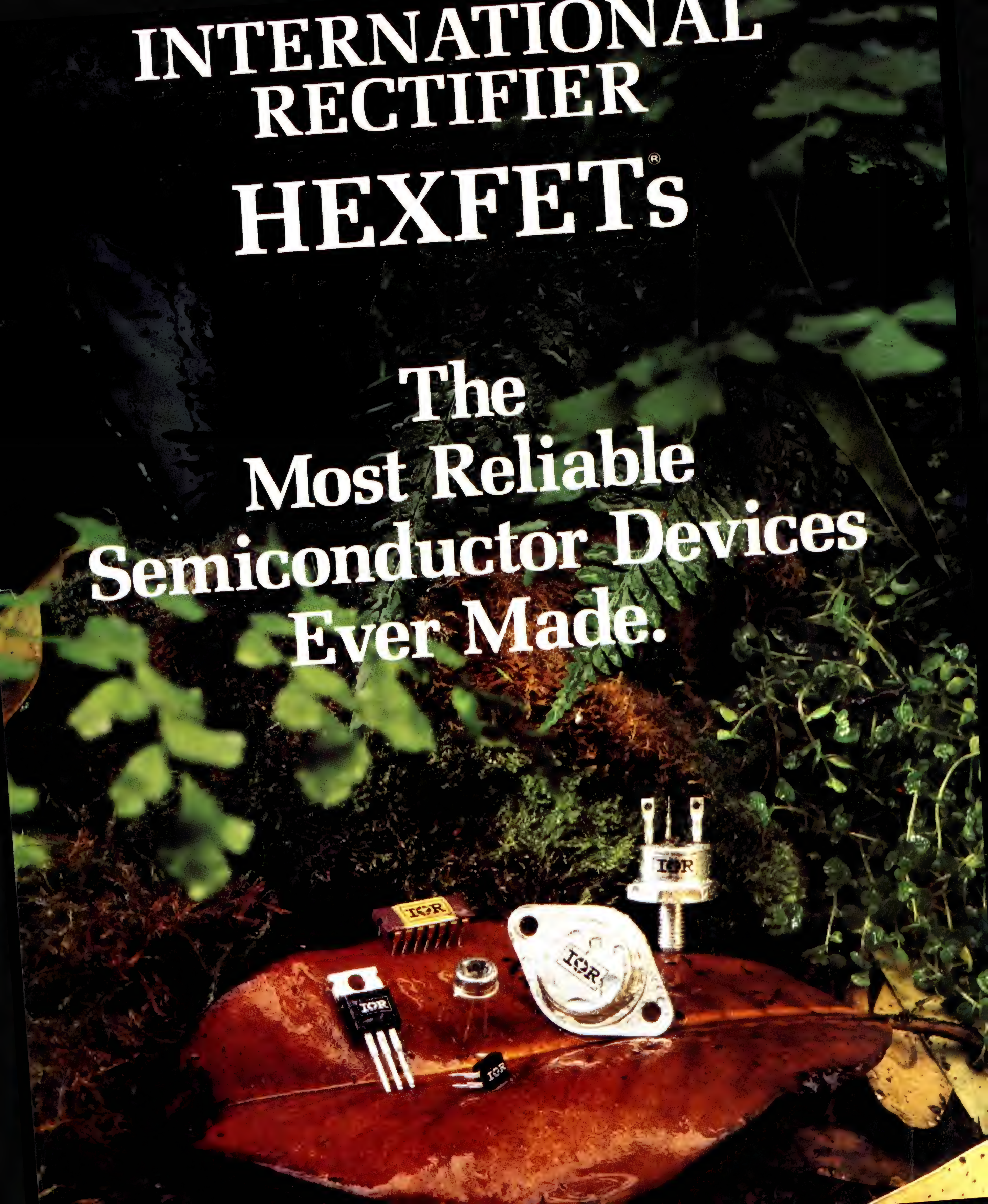
Help for consumer. The idea behind a consumer bus is analogous to that which spawned the RS-232-C standard: to give the user access to any number of electronic products through a single interface. According to Hoffman, the most promising avenue for development lies in the area of remote control, where one controller would link different pieces of home equipment, from personal computers to Compact Disk players. The controller, which could operate by either wire or infrared waves could even be linked to the outside over telephone lines.

At present, the committee is seeking a workable consensus on a standard for the bus. Toward that end, it is soliciting ideas (even very tentative ones) to be sent to Tom Mock at EIA headquarters, in Washington, D. C. In addition, the Engineering Policy Council has sponsored studies by the Georgia Institute of Technology, with the aim of coming up with some proposals for bus design and manufacture.

A number of existing technologies are also being considered—including Philips's I^{2}C serial bus [*Electronics*, Oct. 20, 1982, p. 50]. The European company sees that bus as the de facto standard for communications between chips in consumer and industrial applications.

Hoffman disagrees, saying he is reasonably confident that the industry will fall into line when a standard is announced. The reason, he says, is that the remote-control arena does not have the same strong vested interests as other areas of consumer electronics. He plans to discuss the proposed standard in Chicago at the International Conference on Consumer Electronics, scheduled for June 6–8. –**David M. Weber**

Circle 49 on reader service card →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International Rectifier HEXFETs are beyond ordinary power MOSFETs because they are ***simply the most reliable semiconductor devices ever made.***

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That's the number of device hours our extensive HEXFET Reliability Certification Program has so far racked up in its continuing accelerated testing.

And what do the tests prove?

They prove, for example, that ***all*** HEXFETs consistently exhibit failure rates below 0.6% per 1,000,000 (that's million) hours at $T_j = 77°C$. That adds up to a mean-time-between-failure (MTBF) of more than 20,000 years!

Look at Figure 1. If all the devices in a 1,000-component system were this reliable, you could expect the system to work 20 years without a failure!

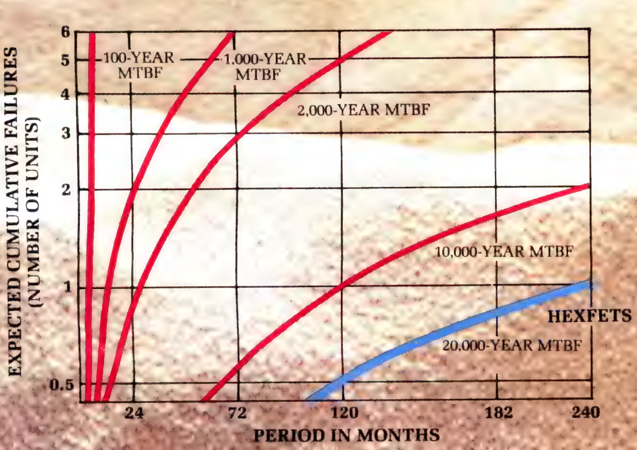

Fig. 1 Expected Cumulative Failures
(Example: 1,000 Component-Count System)

At Last...Predictable Reliability!

When it comes to designing with power MOSFETs, we don't feel you should have to roll dice. Over one-third of our R&D funding is invested on reliability research. That's why we can ***confidently tell you*** what operating parameters to specify to achieve your design life objectives.

For example, based on our results shown in Figure 2, you can now target the reliability of your design by deciding on the junction temperature at which the power MOSFET will operate. Here, at last, is a level of confidence that is truly an industry breakthrough!

And to prove our point, all new HEXFET data sheets will include reliability specs — something you won't find anywhere else.

So why gamble?

There are other equally impressive results summarized in our HEXFET Quarterly Reliability Report (e.g., Figure 3, Expected Failure Rates vs. Applied Gate Voltage and Temperature). Just ask us for a copy. It's free.

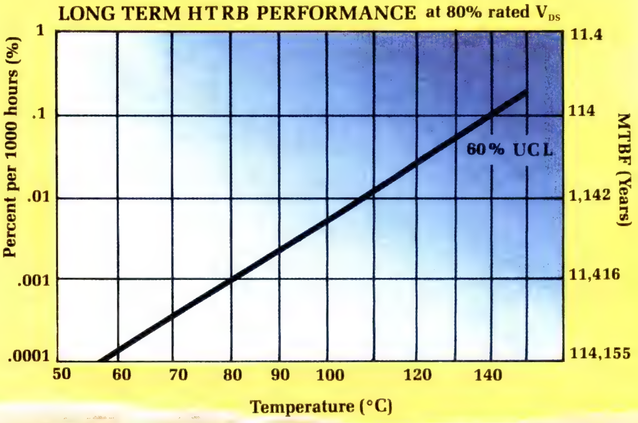

Fig. 2. Life Test Results

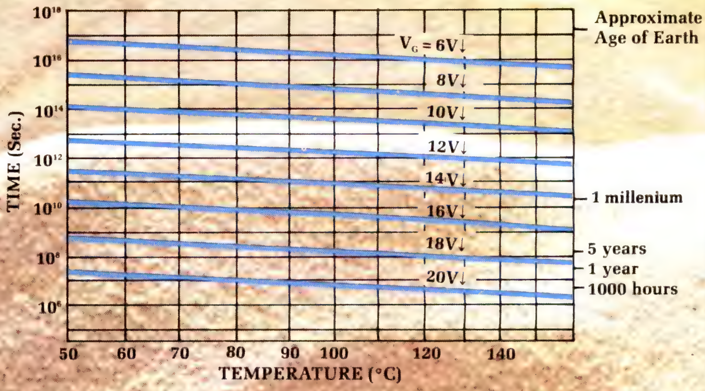

Fig. 3. Time to 1% Accumulated Gate Failures

Infant Immortality!

Early gate failure — the overwhelming cause of infant mortality in power MOSFETs — is virtually non-existent in HEXFETs. Fact is, we've stressed the gates of over 33,000 HEXFETs so far. Result? A total infant mortality currently running at less than 0.08% after two hours at a $T_j = 150°C$, $V_{GS} = +20V$, $V_D = V_S = 0$.

That's just for openers. The following results demonstrate yet another impressive withstand-capability of HEXFETs under repeated power cycling:

Case	No. Devices	Total Cycles	% of Cumulative Failures at Number of Cycles 1Kc	6k	12k	18k	24k	32k	40k
TO-3	185	5.2×10^6	0	0	0	1.2%	3.6%	4.6%	10.6%
TO-220	155	2.2×10^6	0	0	0	1.5%	1.5%	88%	—
HEXDIP	30	8.2×10^5	0	0	0	0	0	—	—

$\Delta T = 70°C$, Cycle Time: 2 to 6 minutes; Failure = > 10% shift in R_{THJC}

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Here's another reason why we don't sell you anything ss than the best for your particular power MOSFET plication.

We put 754 of our plastic TO-220 and 4-pin DIP EXFETs into a chamber at 85°C and 85% relative midity, with a bias of 10 volts applied. To date, more an 1.1×10^6 hours have been logged on TO-220s and ore than 2×10^5 hours on our HEXDIPs.

Total failures? Two. And those were non-catastrophic d occurred at 2000 hours.

ount On Every HEXFET To Perform

Every HEXFET lot manufactured must pass our stringent eliability Certification Program standards — or it doesn't t shipped. And to ensure ultimate reliability, 80 out of each t of 5,000 pieces must undergo a rigorous set of accelerated e tests and process end-point probing destructive tests as own in tables 1 and 2 below.

That's why you can count on superior performance *from ch and every HEXFET you buy.*

Table 1: Reliability Certification — Accelerated Tests

TEST	SAMPLE SIZE	REJECT ON	PURPOSE
HTRB T_j = 150°C t = 12 hours	40	1	Detect temperature dependent failure modes and any change in performance parameters with temp.
GATE STRESS T_j = 150°C t = 2 hours	40	1	Check the reliability of gate oxide and oxides/silicon interface.

Table 2: Reliability Certification — Destruction Tests

TEST	SAMPLE SIZE	REJECT ON	PURPOSE
SOA FAIL POINTS	10	1	Check power handling capability.
GATE DIELECTRIC STRENGTH	10	1	Check oxide integrity.
AVALANCHE ENERGY	10	1	Check ability to handle inductive overloads.
THERMAL RESISTANCE	10	1	Check integrity of header/solder/die interface.

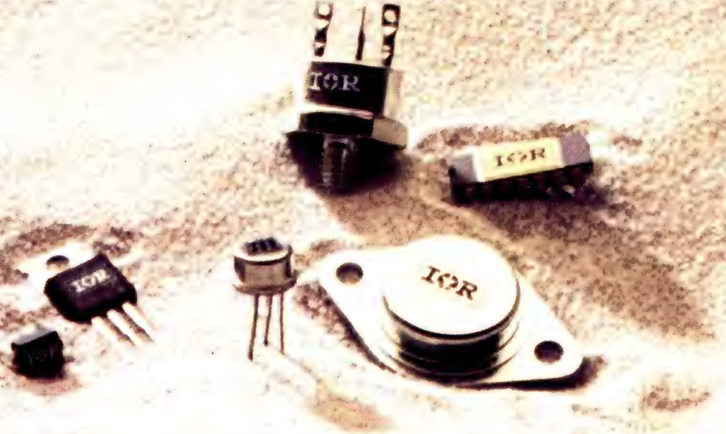
The HEXFET Can't Escape Its Past

Just in case anything *should* go wrong with a HEXFET you can always count on us to help find the reason. We maintain an 80-piece historical stock from every lot we ever produced!

Consider this after-sale story about the validity of our lot traceability.

Four field failures were returned to us for analysis. When compared with devices from the same lot in the historical stock, we were able to determine that the failures were caused by a 52-volt pulse greater than 10 msec between gate and source. We told the customer. They in turn discovered a transient exactly as we had predicted.

Now they place all their trust in us . . . and won't buy power MOSFETs from anyone else.



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We've shipped over 20-billion watts of HEXFET switching power — more than two-thirds of the world's installed power MOSFET wattage.

That alone offers convincing proof of the HEXFET's worldwide acceptance — in performance, cost and, of course, reliability and quality. All these advantages are offered in the widest range of packages and current ratings in both N- and P-Channel versions.

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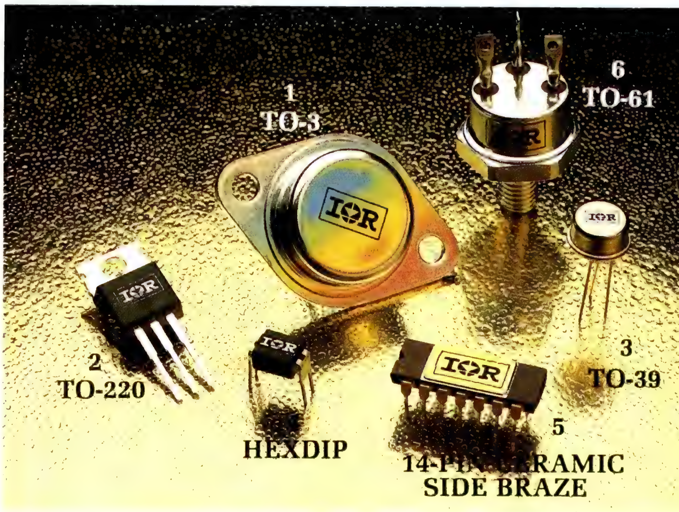

Package Styles	**4, 5**	**2, 3, 4, 5**	**1, 2, 3, 4, 5**	**1, 2, 3,**	**1, 2**	**1, 6**
Chip Size	**Hex Z**	**Hex 1**	**Hex 2**	**Hex 3**	**Hex 4**	**Hex 5**
N - Channel 60 to 100 V	2.4 to 3.2Ω 0.4 to 0.5A	0.6 to 0.8Ω 3.5 to 4.0A	0.3 to 0.4Ω 7 to 8A	0.1 to 0.25Ω 12 to 21A	0.085 to 0.11Ω 24 to 27A	0.055 to 0.08Ω 33 to 40A
N - Channel 150 to 200V	—	1.5 to 2.4Ω 2.0 to 2.5A	0.8 to 1.2Ω 4 to 5A	0.4 to 0.6Ω 8 to 9A	0.18 to 0.22Ω 16 to 18A	0.085 to 0.12Ω 25 to 30A
N - Channel 350 to 400V	—	3.6 to 5.0Ω 1.3 to 1.5A	1.8 to 2.5Ω 2.5 to 3.0A	1.0 to 1.5Ω 4.5 to 5.5A	0.55 to 0.80Ω 8.0 to 10A	0.3 to 0.4Ω 13 to 15A
N - Channel 450 to 500V	—	—	3.0 to 4.0Ω 2.0 to 2.5A	1.5 to 2.0Ω 4.0 to 4.5A	0.85 to 1.10Ω 7 to 8A	0.4 to 0.5Ω 12 to 13A
P - Channel – 60 to – 100V	—	1.2 to 1.6Ω – 2.5 to – 3.0A	0.6 to 0.8Ω – 5 to – 6A	0.3 to 0.4Ω – 10 to – 12A	0.25 to 0.35Ω – 13 to – 16A	— —
P - Channel – 150 to –200V	—	3.0 to 4.5Ω – 1.5 to –1.75A	1.5 to 2.4Ω – 3.0 to – 3.5A	0.8 to 1.2Ω – 5.5 to – 6.5A	0.5 to 0.7Ω – 9 to – 11A	— —

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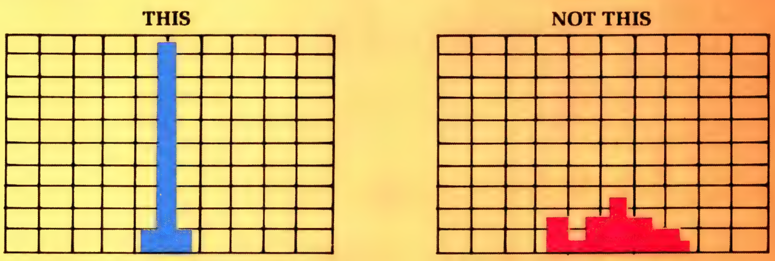
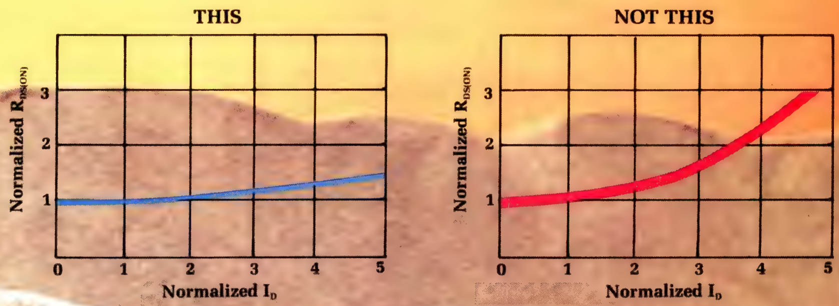
What To Expect From A HEXFET

Because MOSFETs only have one P-N junction and current is handled by majority carriers, they are inherently more reliable than bipolar transistors. To make sure you're getting everything a power MOSFET has to offer, here are some of the things to look for:

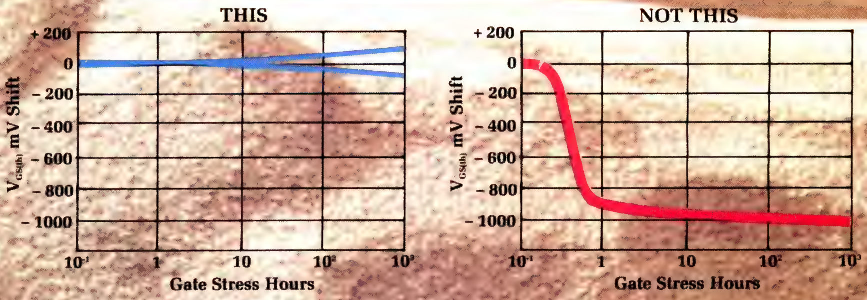
1. Parameter spreads should be tightly clustered, not widely distributed. Tight process control is a requirement for high quality and reliability.



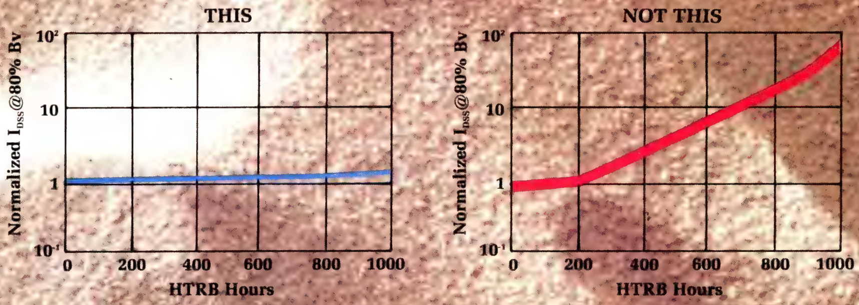
2. $R_{DS(ON)}$ should not increase out of sight as I_D increases, otherwise the ability of the device to handle current surges will be adversely affected.



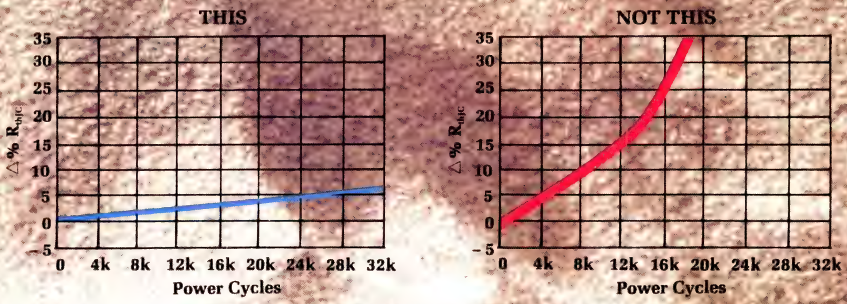
3. Threshold voltage should remain stable on gate stress test. Switching characteristics should not change with time, temperature or applied voltage.



4. Leakage current should be stable on HTRB. Devices should not be prone to runaway.



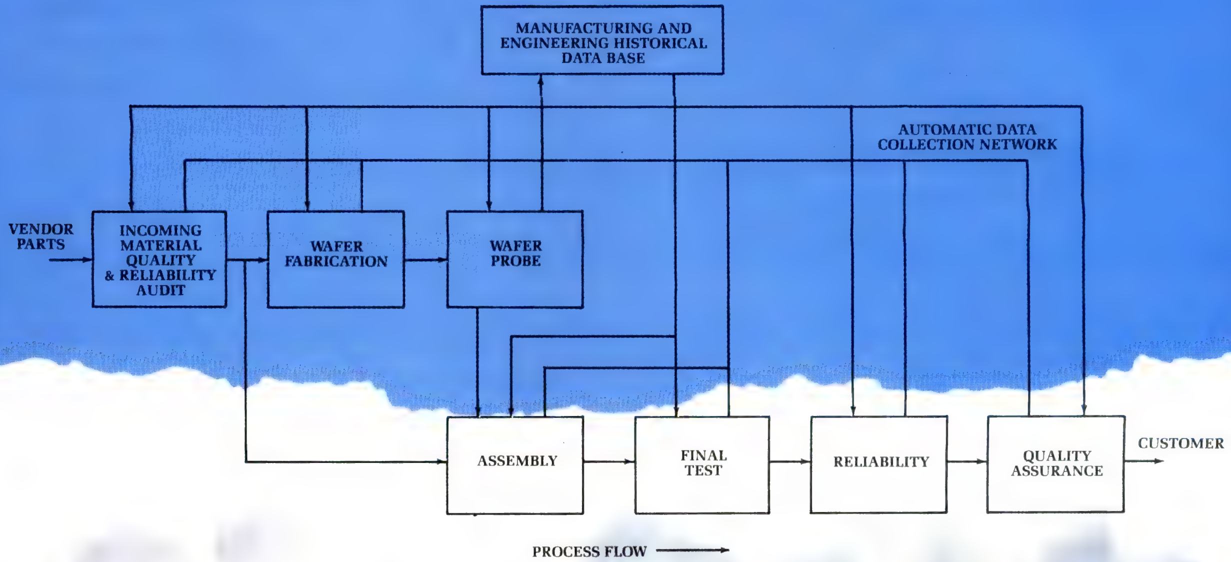
5. Thermal resistance should remain stable on power and temperature cycling.



TQP: The Big Money Saver!

HEXFETs are shipped to an actual outgoing quality level (AOQL) below 200 ppm — consistently! This quality, plus our total lot traceability, has enabled us to offer our customers a Total Quality Partnership (TQP) *ship-to-stock* program that requires absolutely *no incoming inspection* of HEXFETs.

Think of the test equipment, the man-hours, and the inventory dollars you can save!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AUTOMATIC DATA COLLECTION NETWORK
VENDOR PARTS
INCOMING MATERIAL QUALITY & RELIABILITY AUDIT
WAFER FABRICATION
WAFER PROBE
ASSEMBLY
FINAL TEST
RELIABILITY
QUALITY ASSURANCE
CUSTOMER
PROCESS FLOW

Fig. 10: Process/Engineering Feedback Loop ("Seven Sisters")

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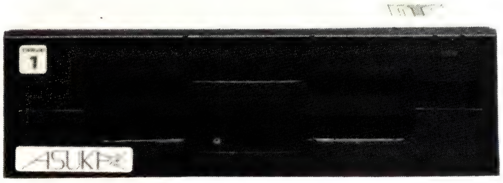

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Washington newsletter

VAN operators to fight phone companies' effort to sell packet switching . . .

Look for the nation's suppliers of value-added networks to challenge the telephone operating companies' efforts to offer packet-switching services for local data transport. The companies have petitioned the Federal Communications Commission for permission to engage in protocol conversion for that purpose. The technical and economic thrust of the operating companies' request raises many unknowns, say the suppliers, that they want hashed out in detail before the FCC takes any action. For example, a spokesman for Uninet, the Lanexa, Kan., firm, says **the numbering and routing schemes proposed by the phone companies are far from compatible with existing packet-switching standards.** "We're all for increased competition, but we don't think overlaying another set of standards on the telecommunications industry is the way to go," he says. Uninet sees the proceeding as an opportunity to get the players to agree on a uniform set of standards once and for all, he adds.

. . . as FCC sees request calling for policy change

For the Federal Communications Commission, the issue goes right to the heart of what its Computer II decision was supposed to do: prevent the telephone companies from distorting costs by commingling regulated and unregulated businesses in the same facility. **"They are asking us to turn our philospophy over on its head,"** remarks Michael Slomin, legal assistant to the chief of the FCC's Common Carrier Bureau. The only way the FCC can decide in the phone companies' favor is if the companies prove the public would incur a net loss without the service, he notes. Local data transport would cut transmission costs to business users by about half and eliminate the need for expensive hardware such as protocol conversion boxes and modems, contend the phone companies.

Computer skills not vital, says science academy

High-school graduates do not need computer skills to succeed in the job market, says a report from the National Academy of Sciences. "Many people assume that advanced technology requires drastically higher skills in computer science and programming; in reality, it often requires lesser skills, especially given rapid improvements in computer self-diagnosis," says the report, sponsored by the academy's Committee on Science, Engineering, and Public Policy. **High-technology industries are growing, but they will employ less than 1% of the work force by 1995, it adds** [see editorial, p. 12]. At the same time, the report concludes that the essential hallmark of upwardly mobile employees of the future will be their "ability to learn and adapt to changes in the workplace."

Congressional study questions Star Wars cost

The Administration's call for $1.8 billion to start a feasibility study of its Strategic Defense Initiative, the so-called Star Wars plan, "excludes many undisclosed costs and is only the beginning of a program likely to exceed $1 trillion and mortgage away U .S. financial and security interests," charges Sen. Larry Pressler (R., S. D.) in reviewing a new report from the Congressional Budget Office. Primary among the reasons to cast doubt on the plan, says the nonpartisan CBO, is the fact that **it excludes the costs of research on many types of technologies, such as the $21.2 million being spent on high-energy lasers** that seem to be critical to it. The office also says funding after 1986 will pick up, rather than slow down as the Pentagon suggests. The program would consume 16% of the U. S. defense budget by 1989 versus about 4% in 1984, notes the report.

Washington commentary

Computer automation's mixed blessings

Computer automation in U. S. manufacturing processes promises better product quality and worker productivity. It also promises a growing job market into the next century for electronics engineers, technicians, computer scientists, upper-level managers, and sales staffs.

That is the bright side of computer automation. The dark side is that it will also mean the elimination of jobs now held by middle- and lower-level managers, craftsworkers, machine operators, clerical personnel, and laborers. Even the number of jobs for computer programmers, on the rise now, will shrink over the long term as more software is converted to interchangeable hardware. Increasing use of programmable automation will aggravate unemployment in heavy industries such as the Midwest's auto plants and the metal-working factories of the Northeast and Middle Atlantic region, as well as the Sunbelt's electronics and aerospace industries. The timing of those cutbacks will be slowed somewhat by the continuing evolution of protoype production packages into marketable turnkey systems, but they will come nonetheless.

These are among the more certain conclusions drawn by the congressional Office of Technology Assessment in its new 471-page study, Computerized Manufacturing Automation: Employment, Education and the Workplace. Copies are available for $14 from the Superintendent of Documents, U. S. Government Printing Office, Washington, D. C. 20402.

Finding money and skills

The OTA suspects that two distinctly human considerations—money and skills—will keep prospective users of computer automation from galloping ahead as fast as they would like with the new technology. Not only will corporate managers first have to identify the systems best suited to their operations; they will also have to find the large amounts of capital that automation will require, as well as to locate workers trained in the appropriate skills. Another initial drawback will be the natural human reluctance of some managements and most workers to alter the status quo.

That time lag will be crucial to a reexamination of educational, training, and retraining issues relevant to automation and the U. S. work force. As the OTA sees it, the U. S. is far behind its competitors—notably Japan and West Germany—in exploring such critical issues as the impact of automation on the work force. The new study urges that educators, employers, labor, and Congress move quickly to reexamine educational, training, and retraining issues in the light of changes to be generated by automation. Fulfilling technology's promise will require "a strong foundation of basic reading, science, and mathematic skills," says the OTA, which sees many prospective workers illiterate in those areas unless the national education system adapts and improves. With an appropriate automation curriculum still to be developed, plus continuing shortages of laboratory equipment and technical faculty, the U. S. education system is not yet ready to deal with the demand.

Corporate candidates for automation need to give as much attention to the human element of job stress in an automated plant as they do to the development of programming standards. That stress comes from "working on very complicated, expensive, and highly integrated systems, and with the lack of autonomy at work, extending in some cases to computerized monitoring [of workers] by management," explains Marjory Blumenthal, OTA project director. Maintenance staffs also suffer substantial stress because of the combination of a complex system and the pressure to minimize downtime because of the high cost of lost production. And purchasers must also design their new operations to discourage excessive boredom and stress that can downgrade worker productivity.

Although U. S. government spending for automation research and development totals $80 million to $82 million this year, the OTA believes that private outlays boosted total spending last year to between $264 million and $400 million for R&D for computer-aided design, robotics, and machine-tool automation. The principal concern about the Federal role is that military agencies are funding 78% of the total, nearly all of it oriented to specific performance goals over the short-term.

Money, however, is less of a problem for automation developers, producers, and users than the need to come up with programs for education, training, and retraining workers. Skilled people who derive satisfaction from what they do are at the heart of the matter. Without people to monitor and maintain them, the machines will not perform. –**Ray Connolly**

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International newsletter

Japan hits first target in fifth-generation computer R&D project

The Institute for New Generation Computer Technology, the organization coordinating Japan's fifth-generation computer research and development project, has achieved the first target in the 10-year program, a prototype relational-data-base machine. The prototype consists of two parts, a data-base processor, manufactured by Toshiba Corp., and a hierarchical memory, made by Hitachi Ltd. to be interconnected with a local network manufactured by Oki Electric Industry Co. The data-base processor includes a supervisory control processor, a relational-data-base engine, a processor to interface to the outside world, and a separate maintenance processor. Later versions will have four relational-data-base engines. **The hierarchical memory subsystem uses 12 megabytes of random-access data-base memory,** two disk drives, each holding 2.5 gigabytes, and two magnetic tape drives. Increases planned are to 128 megabytes of RAM, eight disk drives, and four tape drives.

EC seeks unity in computer interconnects and telecommunications

European Community ministers have asked the European Commission, the executive body of the EC, to prepare concrete proposals for European-wide standards in computer interconnections as a matter of urgency. **A high-level committee will flesh out a four-point program by June 15.** The main objectives are to harmonize EC standards, based on the International Organization for Standardization's reference model for open-systems interconnection; establish a network of test and reference sites for validating different OSI software; set up a number of demonstrator projects; and ensure that maximum regard is given to such emerging standards in government and public-sector purchases. A similar European-wide initiative is to be taken in the area of emerging telecommunications standards such as Integrated Services Digital Network or ISDN.

Toshiba to build its fifth plant within a year

Toshiba Corp.'s aggressive plans to increase its share of the world semiconductor market continue with the announcement that it is beginning construction of a $43.4 million plant that will double its production capacity in discrete transistors. Located in Himeji, near Osaka, **the plant will concentrate on the manufacture of power transistors for the industrial-robot market.** Expected to be in operation by early 1985, it is one of five plants Toshiba either has opened or will open within the next year. The firm's 1983 discrete sales were $405 million.

AEG-Telefunken wins bankruptcy battle, loses ground to competitors

AEG-Telefunken, West Germany's big electrical and electronics producer, finally appears to be over the hump in its long battle to stave off financial collapse. After losses of nearly $350 million in 1982 when the Frankfurt-based company sought court protection from its creditors [*Electronics,* July 14, 1982, p. 80], it registered a net profit of $14 million on sales of $4.27 billion in 1983. With that, **nearly all of the company's eight divisions are now operating in the black.** The firm is well on its way toward making 1984 a profitable year, too, and will definitely meet the September deadline for paying back about $360 million to its creditors. AEG-Telefunken benefited from the general worldwide business recovery during the past year and a half, as well as its own increased productivity and drastic trimming of excess capacity and loss-ridden sectors. Not all is wine and roses, however. While scrambling to recover its profitability, the company slipped to the No. 3 spot (from No. 2) among German electrical and electronics producers, now ranking behind Siemens AG and the Robert Bosch group of companies.

Brazilian protectionism bears fruit for makers of small computers

Brazil's policy of protecting private industry in selected electronics fields appears to be bearing fruit. Preliminary figures released by the Special Secretariat for Informatics indicate that, while multinational computer companies' sales dropped last year in comparison with 1982, **the protected local manufacturers of mini- and microcomputers experienced a sales increase.** The multinational manufacturers—who are allowed to produce and market only large and medium-size computers in Brazil—registered sales of $800 million in 1983, compared with $950 million the year before. Brazilian companies, meanwhile, had sales of $670 million, compared with $558 million in 1982. The study also shows that import restraints and government policies pressing multinationals to use more Brazilian-produced components have also cut into import levels.

Eurotechnique launches smart-card chip

Nearly six months ahead of schedule, Eurotechnique is ready to begin shipping samples of an IC for smart-card applications. Designated the ET 1002 and based on the Intel 8048 microprocessor, the chip meets specifications laid down by Bull and the French Direction Générale des Télécommunications, the country's largest producer and consumer of the cards, respectively. **Both had been receiving a certain amount of domestic criticism for dependence on a single foreign supplier, Motorola.** Smart cards, plastic wallet cards with implanted ICs, were invented in France and are being widely adapted in that country for banking operations and other transactions that require off-line data storage and computing [*Electronics*, Jan. 26, p. 92]. Eurotechnique expects to produce several hundred thousand of the chips, which also include 8-K of programmable read-only-memory, next year. The outfit is the former joint venture of National Semiconductor Corp. and St. Gobain Pont-à-Mousson, since taken over by Thomson-CSF.

Addenda

The French government will provide support for a Thomson-CSF Semiconducteurs IC assembly plant near the city of Nancy. Thomson had nearly decided on Ireland as the site, but **the government stepped in with a subsidy and benefits package to save jobs** in the depressed steel-producing area. . . . **Nippon Telegraph & Telephone Public Corp. will open an office in Los Altos, Calif.,** to handle inquiries from U. S. equipment manufacturers interested in selling to Japan, and to gather technical development information from the U. S. It opened a similar office in New York two years ago. . . . India's state-owned Semiconductor Complex Ltd., Chandigarh, is considering the **establishing a design center in Silicon Valley.** Plans call for the company to use U. S. software and chip engineers to train its own designers. . . . Control Data Corp. and the São Paulo investment bank Brasilinvest are holding informal talks **aimed at forming a joint company to manufacture the 180 series of mainframes** introduced to the U. S. market in April. Brazilian sources have said that they will design supporting software and build compatible peripherals for possible export to the U. S.

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Bistable diodes handle switching in TDM optical system

by Michael Berger, McGraw-Hill World News

To speed communications in digital setups, laser diodes use a light-absorbing layer that acts as an optical flip-flop

The approach of all-digital communications systems has brought with it the demand for ever-faster switching, which makes the news from Japan's NEC Corp. particularly good. Researchers there have successfully used bistable diodes for optical time-division-multiplexed switching.

A previous NEC device, developed last year for the same function, used single-mode optical-fiber lines to delay signals and achieve time-division switching. The major drawback was that the fiber lines could not regenerate or amplify signals.

"It is like being on a freeway and being able to travel at very high speeds and then having to slow down because of congestion at the interchange," says Teiji Uchida, vice president of the Optoelectronics and Laser Device Research & Development groups. "That is the problem we face in developing optical switching: to see that the line speeds which we already can achieve can be maintained through switching systems as well."

This latest system, which NEC will present at the Congress of Laser Electronics Organizations, June 19–22 in Anaheim, Calif., uses a 1.3-micrometer indium gallium arsenide phosphite loss section sandwiched between two gain sections. The loss section acts as a light-absorbing layer, being highly attenuative when a weak input signal is applied but turning hysteretic when the signal is strengthened.

Each bistable laser-diode module is composed of the laser chip, two coupling circuits (one of which is a hemispherical graded-index rod lens), a single-mode fiber, and a polarization-maintaining fiber. Coupling losses between the laser diode and the fiber circuits are between 4.0 and 4.4 decibels. The laser-diode modules are connected with integrated optical waveguide write/read switches fabricated on a niobic acid lithium chip.

When an optic input signal of 30 microwatts is applied to one electrode, it is slightly amplified through the gain sections and absorbed by the loss section. When the signal is strengthened, the loss section becomes "transparent"; the laser diodes begin oscillating rapidly; and the original input of 30 μW is amplified to an output of 3 milliwatts.

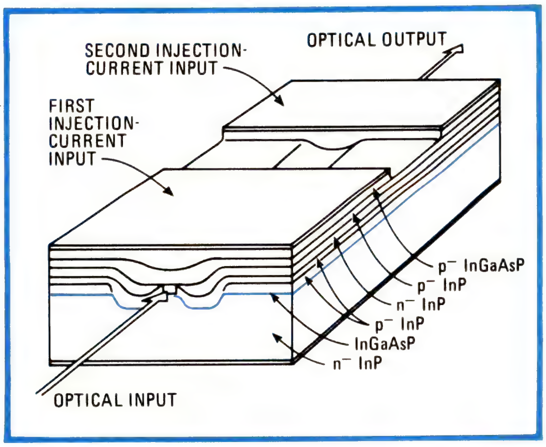
When the optical input is turned off, the light-absorbing loss section retains the 3-mW signal, thus providing a memory function. An electrical reset pulse applied to one electrode stops the oscillation. The laser diode requires a minimum optical input power of 9 to 12 μW for memory set operation. Optical delay time is 4 to 5 nanoseconds.

In the NEC experiment, teams from the Optoelectronics Research Laboratory and Computer & Communications Systems Laboratory, Kawasaki, multiplexed four 8-megabit TV-camera signals into a 32-Mb-per-second pulse stream and then converted it into an optical signal that is then demultiplexed and fed to the four bistable laser-diode modules.

Fast work. The modules store and then switch each signal in time-division sequence. The four optical signals are multiplexed again, reconverted back into an electric signal, demultiplexed, and transmitted to their respective TV monitors. Total time for the entire operation is 1 ns.

"This is only a start," says Uchida, noting that optical switching will have two major merits: a very wideband switching capability for TV signals, plus the virtual elimination of cross-talk, a big drawback of present high-density packet switching.

Within five years, Uchida predicts, optical switching for line-transmission speeds of 1.6 gigahertz per second will be achieved for local networks. Developing this technology for public exchanges, he says, would probably take 10 years, "but who would have



Light sandwich. NEC laser diode uses a 1.3-micrometer indium gallium arsenide phosphite loss section, sandwiched between two gain sections, to act as a light-absorbing layer.

thought 10 years ago that fiber-optic cable would eventually replace all underground and undersea communications cable?"

The next research tasks, he says, are to lower power consumption (now 80 kilowatts using a 2-volt power supply) and improve switching speed to 0.5 ns.

Computer-aided design

Systems engineers to design VLSI chips

With integrated circuits approaching the complexity of systems, it makes sense for systems engineers to take on the task of IC design. Acknowledging this fact of life is Ing. C. Olivetti & C., which is establishing a center at its Ivrea, Italy, headquarters where the engineers from its systems divisions will design very large-scale ICs for use in its entire range of products, from electronic typewriters right through minicomputers.

"Our primary objective is very simple," explains Tito Conti, Olivetti's manager for production and quality control. "It is impossible to optimize product solutions using standard commercial ICs, so we're trying to diffuse IC design know-how throughout our systems divisions."

Simple, too, is the motivation for doing so. With the advent of VLSI technologies and resulting systems on a chip, more of the value-added in electronic systems resides in the components.

While that might be an acceptable situation for a vertically integrated corporation with its own component-production facilities, it puts the pure systems manufacturer in a vulnerable position. So Olivetti is taking advantage of a parallel advance in IC design software to keep that value added in-house. The company expects to see others follow its lead.

Software help. The design center was conceived with the cooperation of VLSI Technology Inc., San Jose, Calif., a company in which Olivetti holds a 40% interest. That acquisition was part of the Italian firm's venture-capital program, aimed at plugging what it considered potential holes in its product line and production facilities. Olivetti was attracted to VLSI Technology because of its original software based on Mead-Conway principles. This "correct-by-construction" approach, which requires no knowledge of semiconductor technology, is considered ideal for furnishing IC design tools to systems engineers.

The Olivetti design center can handle 10 designers working at any one time, though in the beginning, at least, its training activity will be as important as its design production. Essentially, the designers will be learning to work backwards from system requirements to create, say, block diagrams of system cells, from which the software can in turn generate a layout.

Other essential help from the software takes the form of automatic adjustment of circuit capacitance and speed from requirements furnished by the designer. Likewise, a logic diagram of the various cells of a circuit is the only input necessary for generation of its routing. The contract between VLSI Technologies and Olivetti provides for an updating of the Italian company's software as the U. S. company develops new and improved tools.

Satellite link. The center is equipped with Apollo work stations driven by a Digital Equipment Corp. VAX 11/780 computer. Completed designs can be transmitted by a dedicated satellite data link to VLSI Technologies, whose side of the contract guarantees it a role as a silicon foundry for a certain quota of the ICs for a period of "several years." Beyond that quota, Olivetti can furnish the tapes it generates to any IC manufacturer for fabrication.

After five to seven weeks, samples of the circuits produced in either 2.5-micrometer high-density MOS or 3-μm complementary-MOS will be returned to the design center for testing and physical verification by scanning electron microscope. When the required parameters are satisfied, the design will get a production go-ahead. **–Robert T. Gallagher**

Designed for design. Olivetti's center at Ivrea, Italy, will give engineers from its systems divisions the opportunity to design VSLI chips for use in its entire product range.

Speech

Chip and board go Forth and talk

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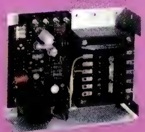

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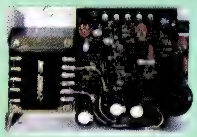

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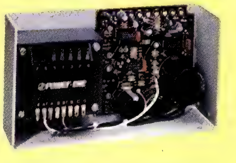

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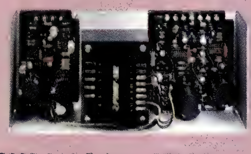

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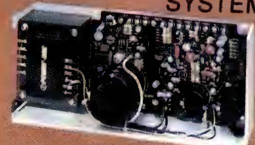

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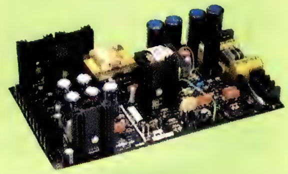

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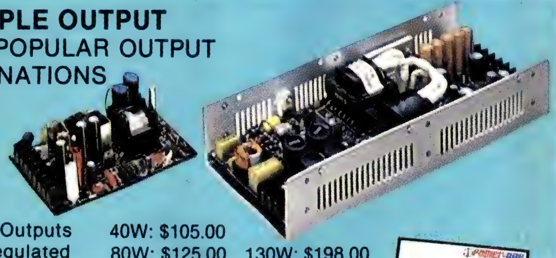

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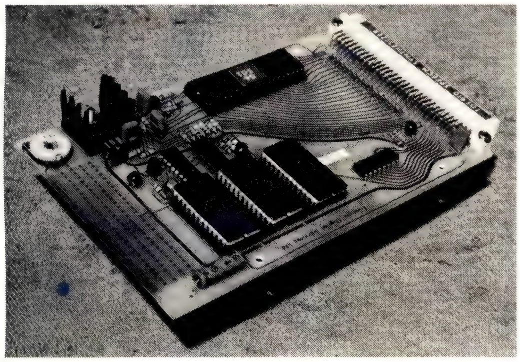
nounce the time of day, what buses are using that stop, and when they are due.

When a bus is running off schedule, inductive loop sensors buried in the road interrogate circuitry in the bus cab to identify it. The microprocessor controller in the speech synthesizer scans the sensor, detects the oncoming bus, and a voice will announce something like, "The bus now approaching is a No. 10." Meanwhile, the controller figures out when the next one is due.

London-based Triangle Digital Services Ltd., a one-man outfit set up by Peter Rush, developed the prototype hardware for the system. Formerly a product manager with General Instrument Microelectronics Ltd., Rush set up shop to provide a systems service to potential users of voice systems.



Talkative. Triangle's speech-synthesizer board consists of (clockwise from top) the TDS90 speech-synthesizer chip; standard DIN 41612 connector; interface for serial EIA inputs, binary parallel handshaken signals, or 1-of-16 switched signals; decoder for additional speech memory; 16- or 32-K E-PROMs or ROMs for speech memory; spare user matrix (blank area); analog conditioning and amplifier; pitch adjustment; and on-board power-supply regulation.

He has developed a custom speech chip using a digital logic array. This is mounted on a self-contained Eurocard-sized board. To go with it, there is a Forth-language microcomputer board. Rush says he chose Forth because its high-level-language capability speeds development work.

Using the speech-synthesizer board and the microcomputer board (which serves as its own development system), Rush can quickly meet a customer's requirements, even tailoring the voice to the application. For Britain's National Physical Laboratory, for example, Triangle has developed a handheld keypad with 16-digit alphanumeric display. It is used to check readings as they are entered into the laboratory computer. With the synthesizer speaking in a brisk manner with truncated ennunciation, it can keep up with the user as he keys in a long number string.

The terminal can be used both for entering data and instructions and for receiving prompts from the laboratory computer. For example, it could give the operator a cue about what reading to make next or indicate that a reading is out of range. The terminal communicates with the laboratory computer systems through an RS-232-C interface at 9,600 bits per second or through an IEEE-488 port.

Triangle has now acquired the rights to the terminal from NPL and is also negotiating with the Department of Transport for the rights to the passenger advisory service, which clearly has potential applications in road, rail, and airplane terminals, just for starters.

For those companies with sufficient expertise to assemble their own systems, Triangle also sells its various board products directly. One is a speech-syn-thesizer board that can be operated directly from relay contacts, asynchronous links over twisted pairs, or parallel binary-coded decimal inputs.

Forth talk. Triangle has also developed a Forth development board based on a Hitachi 6303—a complementary-MOS variant of a Motorola part—and running Triangle's own Forth system. The board is a useful tool for real-time applications, since multitasking programs can be written in a high-level language.

Moreover, users can extend the language as they go along, building their own expertise into their systems. Rush has used this feature to develop progressively more sophisticated speech-control algorithms. The result has been speech with very acceptable quality.

The Department of Transport system shows off the microcomputer's multitasking capability. First, it keeps a calendar that tracks the minute, hour, day, and month. It responds to changes in summer and winter schedules and switches to the appropriate timetable.

Second, it scans the inductive loop sensors and decodes the detected signal. Next, it controls the speech-synthesizer chip's vocabulary and adjusts the volume to compensate for ambient noise levels. "The lady shouts when a lorry goes by," says Rush. There is also a switched-capacitor-filter board with a 12-decibel-per-octave cut-off. **–Kevin Smith**

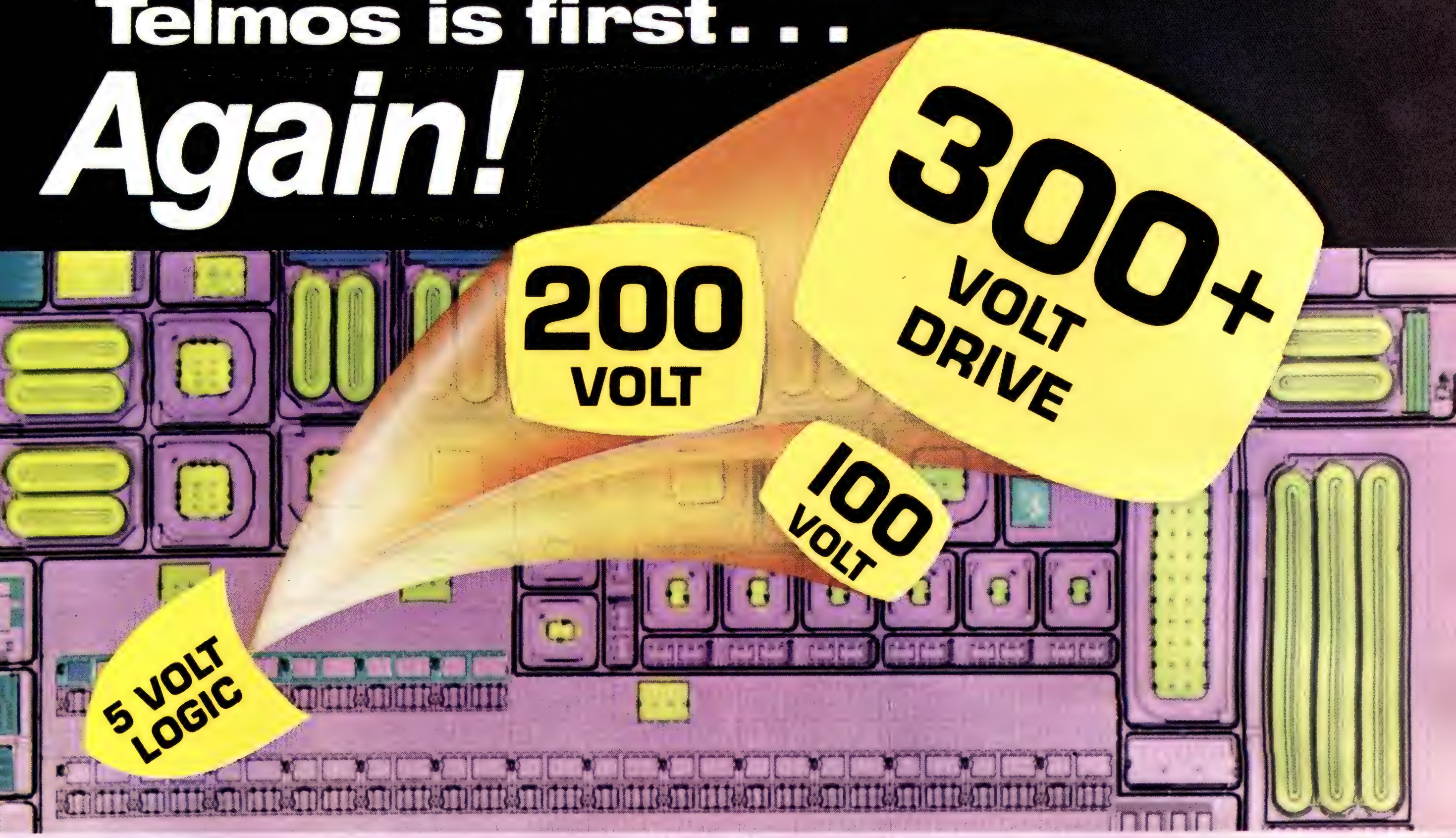
Computers

32-bit superminis next Brazilian target

Brazil's nationalistic Special Secretariat for Informatics has given three groups proposing to develop 32-bit superminicomputers in-house the go-ahead, while proposals by five others who want permission to buy technology from abroad are "being analyzed, with no date for a conclusion," says a secretariat spokesman.

The three groups that will each develop their own superminicomputers are Cobra Computadores e Sistemas Brasileiros SA, Rio de Janeiro; Labo Eletrônica SA, São Paulo; and SID Sistemas de Informação Distribuída SA, Curitiba. All currently manufacture 16-bit minicomputers, which are already subject to protectionist legislation in Brazil.

The five other groups are seeking to work with companies in the U. S., France, and Japan. Edisa Eletrônica Digital SA, in the southernmost state of Rio Grande do Sul, proposes to base its superminicomputer on a Fujitsu model. Digital Equipment Corp. technology is sought for a group formed by Bradesco Banco Brasileiro de Descontos SA, the country's largest bank, and the Companhia Docas



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de Santos, an electronics group—both of São Paulo—together with Medidata Informática e Tecnologia SA, a Rio de Janeiro computer and software company.

Itaú Tecnologia SA, São Paulo, a subsidiary of the Banco Itaú SA, wants to base its superminicomputer on a machine from FIS Inc., a subsidiary of Formation Inc., Mt. Laurel, N. J. The Formation machine is compatible with the IBM 4300.

Sisco Sistemas e Computadores SA, a São Paulo minicomputer manufacturer, wants its superminicomputers based on machines out of IPL Systems Inc., Waltham, Mass. Finally, ABC Sistemas SA, part of a major electronics group in the state of Minas Gerais, plans to use DPS6 supermini technology from France's Bull. Another company from the same group already makes mainframes with Bull technology.

The secretariat's spokesman says that applications from the five companies seeking foreign technology are still being considered. But the feeling was that it would be better to authorize the three in-house developments now, since their projects will take longer to bring on line.

It may be doubted whether the Brazilian market has room for more than three superminicomputer manufacturers. The market is estimated at 2,500 machines, representing sales of about $1.5 billion, over the next five years.

–**Rik Turner**
McGraw-Hill World News

Business

Labor unrest, poor government planning may end semiconductor boom in Philippines

The labor-intensive electronics industry in the Philippines has become, in the last few years, the country's largest dollar-earning industry, mainly because it capitalized on the presence of abundant manpower. In its most profitable period a year or two ago, the industry earned more than $1 billion from exports, according to the Ministry of Trade and Industry, eclipsing such traditional exports as sugar and coconut oil.

But the Philippines' electronics boom, especially in semiconductors, looks to be shortlived. The country may have missed the boat, as other competitive Asian countries like South Korea, Taiwan, Singapore, and Hong Kong have moved into high-technology electronics or to automation in the production of semiconductors. Problems with labor also pose a threat to the electronics sector (see "Philippines has labor pains").

Among the reasons for this failure to move ahead, according to representatives of foreign semiconductor firms, are planning deficiencies and lack of direction. Vicente Chuidian, chairman of Dynetics Semiconductors Inc. and president of the Philippine Association of Electronics Exporters, blames the government's lack of a systematic and responsive program to promote exports in the face of the continuing surge in worldwide demand for semiconductors. He suggests, for instance, that the government reexamine its present strategies for developing exports and establish a well-thought-out, coordinated, long-range plan in consultation with the private sector. Chuidian also emphasizes the transfer of technology as necessary in developing exports.

Although semiconductor manufacturers are still able to get needed materials and supplies, such as components and parts for local assembling and packaging, a financial crisis, caused by a widening balance-of-payments deficit and shortage of dollars [*Electronics,* Jan. 12, p. 76], has resulted in cash-flow problems and is discouraging expansion and sales.

Moreover, U. S.-based companies have either scaled down their output in the Philippines or have opted for expansion elsewhere in Asia. Advanced Micro Devices Inc. is expanding its operations in Malaysia, while Texas Instruments Inc. is buying 30% of the output of Anam Semiconductors of South Korea. Zilog Inc. reduced its Philippine operations, and Signetics Inc. ceased operations altogether last year.

Local firms like Stanford Microsystems Inc. and Dynetics, which were doing extremely well by servicing the requirements of foreign buyers, have been as disenchanted with future potential in the local industrial environment, as the foreign corporations have. A number of these local firms have announced they will be building new plants outside the country.

–**Bernardino Ronquillo**
McGraw-Hill World News

Philippines has labor pains

The Philippines' semiconductor industry, now the country's largest single dollar earner, may lose its premier position in the economy unless it can deal satisfactorily with restive labor unions seeking higher wages under bargaining agreements being renegotiated before they expire. In order to forestall any disruption that could worsen the country's dollar problem, the Ministry of Labor and Employment is seeing to it that unresolved labor disputes are certified to the National Labor Relations Commission for compulsory arbitration. It has just certified a dispute between labor and management at Stanford Microsystems Inc., where talks have bogged down. Labor minister Blas Ople says that if the strike should force a Stanford plant to shut down, the company would stand to lose $4.8 million a month, and the country would be deprived of about $35 million annually in export earnings. Some 7,000 Stanford workers would be idled. The company is reputedly one of world's largest electronics subcontractors, and as an independent Filipino subcontractor, it operates the biggest semiconductor plant in country.

–B. R.

People

Uchida charged with shaping NEC's optoelectric future

"The work of our industrial engineers is to think of what is needed today and tomorrow," states Teiji Uchida, vice president of NEC Corp.'s Optoelectronics and Laser Device Research & Development groups, in Kawasaki. "The work of our R&D group is to think of the day after tomorrow."

Uchida, a former microwave engineer who turned to laser research in 1960 when commercial laser technology was introduced, was talking about NEC's recent announcement of its successful experiment using bistable laser diodes for optical time-division switching (see p. 65). "It will be 10 years before the full development of optical switching, but this is a promising start," he says.

Uchida says that other firms have followed NEC in experimenting on optical-exchange systems, and interest in Japan "is already at the conference-session level." At the annual convention of the Japan Institute of Electronic and Communications Engineers, in March, 15 papers on optical switching were presented—three of them by NEC teams from the Optoelectronics and Computer and Communications Systems research laboratories.

When Uchida first began working on gas-laser and optical-modulation research in NEC's laboratories more than 20 years ago, he was one of a staff of only five. Today, the 53-year-old graduate of Tokyo University oversees almost 400 people, "and we are hiring 20 to 30 additional engineers each year" for optoelectronics.

He became an administrator as well as a researcher in 1976, when he was appointed general manager of the Electronics Research Laboratory. He also headed the Optoelectronics Research Laboratory, which was organized in 1980.

Uchida became a vice president of the company last year, when he assumed responsibility for a growing share of the company's overall R&D budget of almost $300 million a year. He says that in fiscal 1983, NEC spent about $60 million for basic research on such problems as time-division optical switching.

Sees the light. Teiji Uchida has made a promising start NEC's vast effort in optical-electronics research into commercial realization and profitability.

"It is much too early to say which of the many approaches to achieving reliable optical switching will be best," he says. "For example, space-division switching is a possibility, but there is a tendency toward time-division switching, and we hope that our work will stimulate competition. Without competition, there cannot be progress."

Microvitec's Antony Martinez is on the fast track to success

Antony Martinez has gone far and fast in the last five years. Back in July 1979, he set up Microvitec plc, Bradford, Yorkshire, to produce low-cost color monitors for the microcomputer market. Today, the 54-year old Martinez is chairman and managing director of a fast-growing company with $14 million in sales and 200 employees.

In April, Microvitec won one of UK industry's highest accolades—a Queen's Award for Technological Achievement—for the development of its Low Complexity Color Display—basically, a bare-bones chassis of modular design, using interface cards to equip the unit for different applications. The display can be manufactured at low cost on high-volume assembly lines, making it quite attractive economically. Today, Microvitec can boast the UK's fastest-selling low-cost monitor and was recently chosen the sole supplier under a government program to provide microcomputers to all primary and secondary schools.

"We are now doubling capacity eightfold and that is before we add our new facility," says Martinez. Meanwhile, the company is expanding its product line, selling switched-mode power supplies and floppy-disk assemblies. A subsidiary company, Microcolor Graphics Ltd., has been set up to market professional graphics terminals using the same low-cost monitor chassis.

It is all heady stuff, but Martinez bears it with an aplomb acquired during a professional lifetime of wide-rang-ing industrial experience. Born in Malaga, in southern Spain, he first came to the UK in 1950 to study telecommunications and electronics in London. Afterward, he began a busy professional career, working for both consumer and professional electronics companies, which included GEC-Marconi Electronics Ltd., Peto Scott Ltd., and a small design consultancy. Eventually, he ended up as chief engineer of the Bradford production unit of Radio Rentals Products Ltd.

Starting small. In only five short years, Antony Martinez has taken his start-up to a multimillion-dollar award-winning company.

Then, in 1974, Martinez joined Texas Instruments Ltd., finally becoming European consumer-products manager. "When I moved there, I was short on marketing experience and a little raw on human relations," he remarks. At TI, he filled both gaps. "I was putting together proposals for new projects. I had to forecast what was going to happen and I really enjoyed it." ☐

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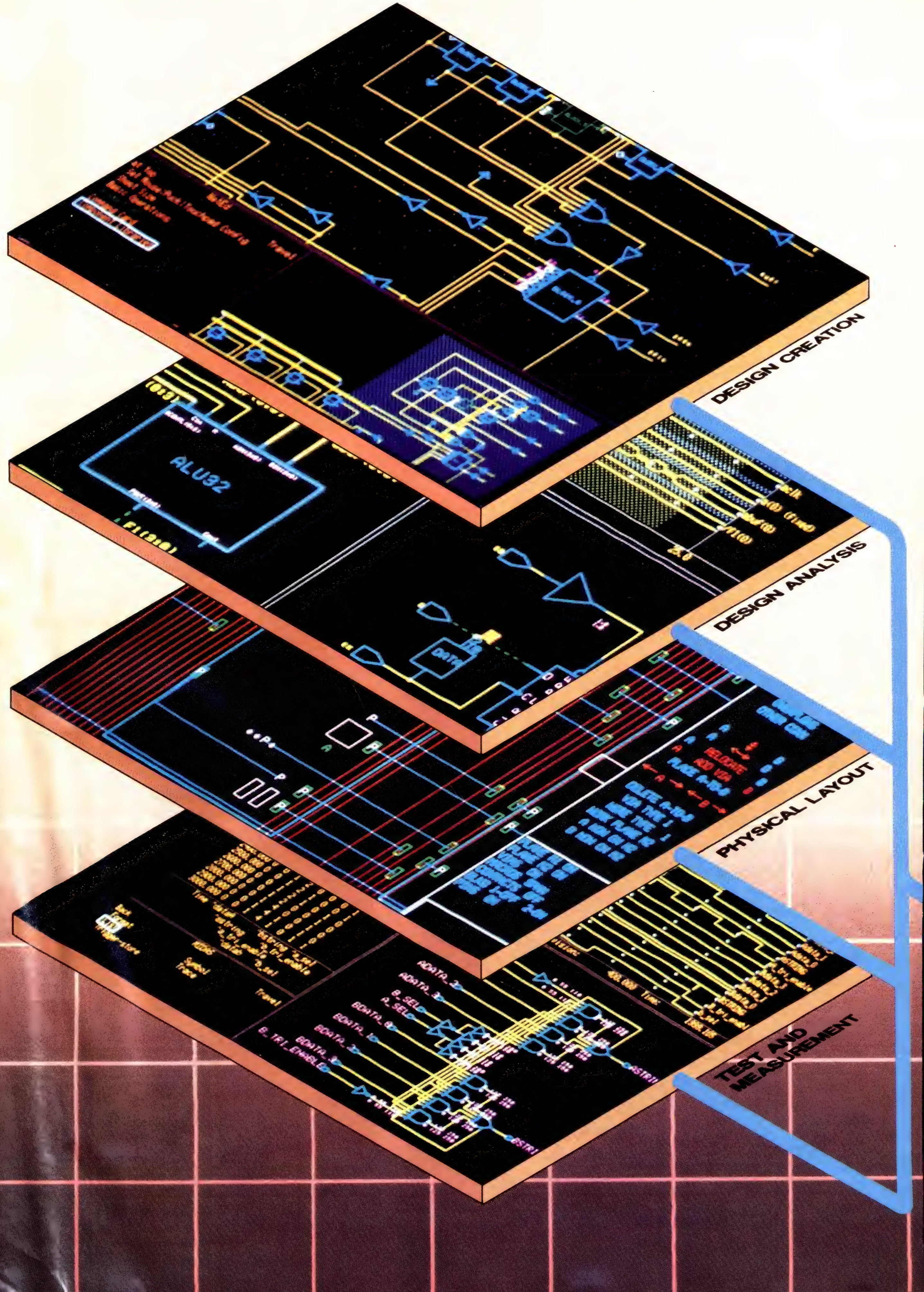
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Circle 132 on reader service card

Printers meet competition head to head

by Robert Gallagher, Paris bureau manager

Five desktop units range widely in price and capabilities, so uses could extend beyond computer line they accompany

If anyone doubted the seriousness of Ing. C. Olivetti & C.'s assault on IBM Corp.'s commanding position in the personal computer market, those reservations should be laid to rest by a new family of aggressively priced printers the Italian company will be marketing to accompany its new M 21 and M 24 Personal Computer-compatibles [*Electronics,* April 5, p. 63]. Moreover, these units are available with serial and parallel interfaces, so their potential market will almost certainly be larger than the one for the company's new personal computers.

Designated the PR family, the line consists of five desktop printers that range in price and performance from an inexpensive model for the most modest personal configurations to a high-speed dual-definition machine that can hold its own against much more cumbersome competition. Four of the printers are based on dot-matrix printheads; the last offers letter quality with a daisy wheel.

At the bottom of the line is the PR 15, a 120-character/s bidirectional printer that offers two levels of print quality for just $500. The PR 15 prints double-width or correspondence-quality output using a nine-needle ballistic head and (like the three other dot-matrix printers) can offer a graphics capability and a character set in 13 national variants, according to the company.

Customers who need a wider print field than the PR 15's 8-in. one can move up to the PR 17, which for about $1,000 will offer a 13-in. field with precisely the same drive characteristics. The next step up is the PR 19, which uses the same printhead as the PR 17 but more than doubles the printing speed, to 300 characters/s. In addition to the standard printing mode, the PR 19 can do double-width printing and a letter-quality printing that works at 150 characters/s. Although Olivetti has not yet set the price for the machine, it is expected to cost less than $2,000.

Top of the line. The Rolls Royce of Olivetti's new line is the PR 1580, a 13-in. dot-matrix printer that offers three variations on data-quality output at a blazing 480 characters/s and four possibilities for near-letter-quality printing at speeds that range from 100 to 150 characters/s. In addition, the PR 1580 uses its 9-by-9-dot-matrix printhead to hammer out pica, elite, mikron, or proportional fonts and can deliver four copies simultaneously. At a price of around $3,000, Olivetti expects to sell at least as many of these machines for professional applications as it will for personal computer use.

The line is completed by the PR 340, a 13-in.-wide daisy-wheel printer that produces letter-quality output at 45 characters/s. Its price will lie between those for the PR 19 and the PR 1580.

All the printers have transmission rates as high as 9,600 bits/s and a choice of serial or parallel interfaces—RS-232-C and Centronics, respectively—with either Olivetti or Diablo command codes. In addition to standard rear-feed paper controls, a sprocket and automatic sheet feeder are available as options.

The printers are slated to go into production soon and should be available within two months.

Ing. C. Olivetti and C., 77 Via G. Jervis, 10015 Ivrea, Italy [Circle reader service number 441]

Single IC carries two audio amplifiers, cuts parts count for walkaround sound gear

An integrated circuit that puts out 150 mW with no external components, not even speaker capacitors, enables makers of miniature audio systems to further reduce equipment size. The TDA7050T, from the Philips Electronic Components and Materials (Elcoma) division in Eindhoven, the Netherlands, uses several patented schemes to cut the component count and current consumption.

The IC is small enough to fit into miniature gadgets, tiny radios, and even watches. Yet it produces sound quality high enough to be used in top-of-the-line walkaround cassette players, the company claims. The TDA7050T needs no ripple capacitor, no feedback loop (which saves four resistors and two capacitors), no bootstrapping (another two capacitors saved), and no external filter (which eliminates still another capacitor and a resistor). Also, the high output power allows the use of low-efficiency headphones, which results in a further cost saving.

The IC consists of two amplifier circuits and can provide either monophonic or stereophonic sound. The outputs can be connected in a bridge-tied load (BTL) configuration, and the signals fed to a single loudspeaker to give a 150-mW mono output. Thus two ICs provide two stereo channels, with no need for speaker capacitors; alternatively, a single IC will give two 35-mW stereo channels. The outputs are then connected to the headphones through the usual speaker capacitors.

Four stages. The TDA7050T has four stages: an input stage with a voltage-to-current converter, a current-summing amplifier, a current-to-voltage converter, and an output stage. The input stage features accurate transconductance due to the high gain of the input-transistor configuration. It converts a differential input voltage into a current then fed to the current-summing amplifier.

The class-AB output stage contains two complementary transistor configurations that act as single npn and pnp transistors with very high current gain. This circuit's output is fed back into the current-summing amplifier for current-to-voltage conversion. The high current gain of the output-transistor configuration makes an on-chip Miller compensation circuit very effective. The high-efficiency output stage is very stable, meaning the output needs no compensation network.

The IC's quiescent current is less than 4 mA, and the supply voltage may range from 6 V down to 1.6 V,

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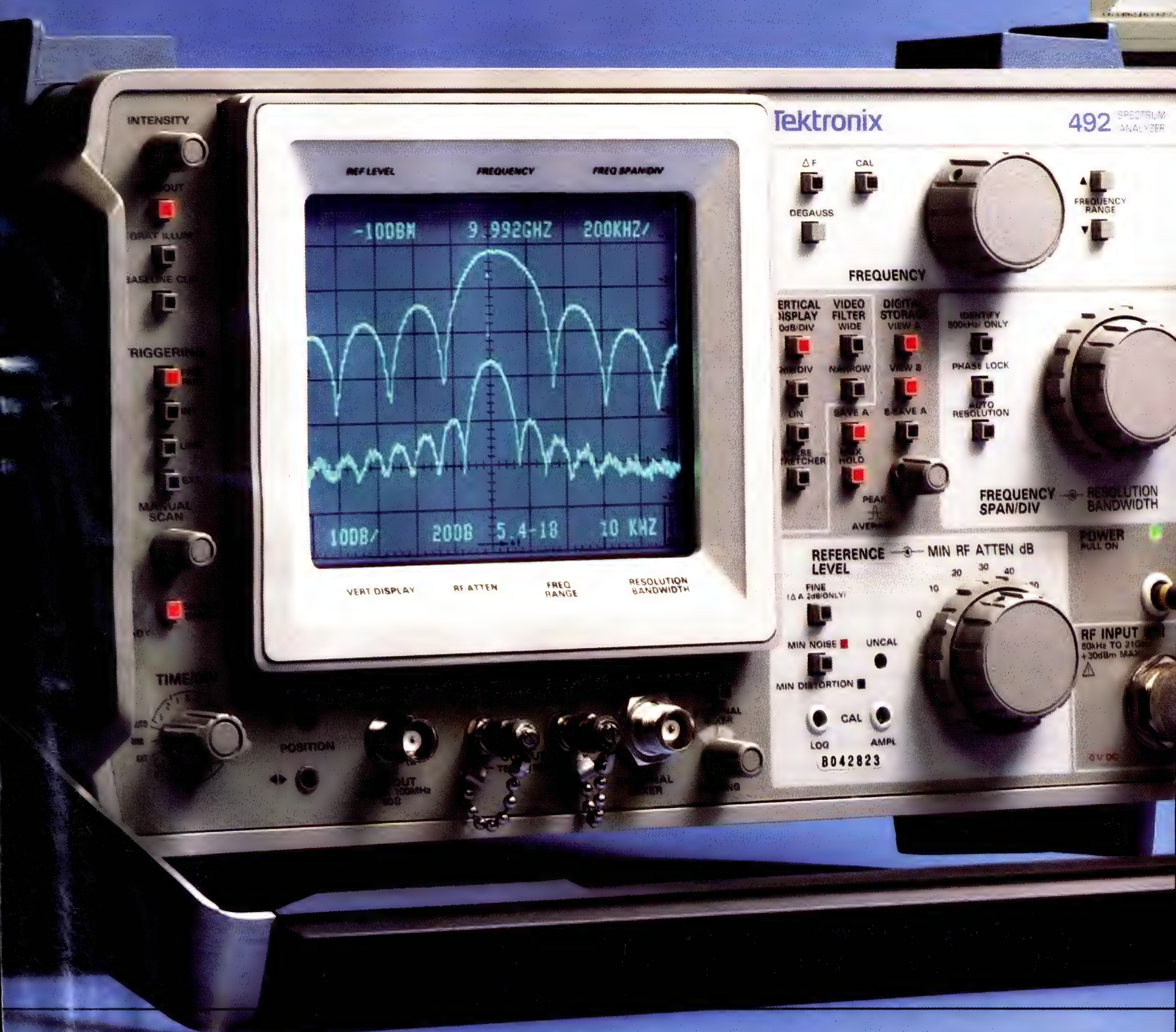

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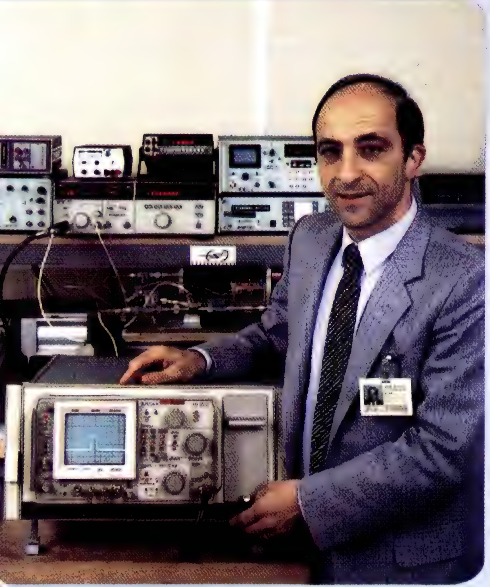

Mr. Marcel Geller,
Manager, Instrumentation Labs Group,
Electronique Serge Dassault, Paris.

"We require high performance of a spectrum analyzer in a variety of applications, in the lab and on board aircraft. For us, in many applications, the only instrument that now meets our requirements is the Tek 492."

"The 492 has provided us those benefits which we need most, especially portability and broad frequency range," says Mr. Marcel Geller, Instrumentation Labs Group Manager, Electronique Serge Dassault.

Electronique Serge Dassault is one of France's leading advanced electronic equipment companies, its extensive product line ranging from airborne radars and homing heads for missiles to road traffic control systems and automated bank tellers.

Mr. Geller, who heads the firm's instrumentation services group and one of the most sophisticated calibration labs in France, and who reviews all new equipment requests, explains, "Our decision to purchase the 492 was based on capability and technical specifications and, of course, the price—all relevant to the problem we had to solve."

Other spectrum analyzers would have meant settling for less: Less frequency coverage. Less convenience.

The 492 has the widest amplitude calibrated range of any spectrum analyzer available: 50 kHz to140 GHz using Tektronix external waveguide mixers. Other commercially available mixers provide frequency calibrated coverage to 220 GHz. The 492 features 80 dB on-screen dynamic range, high resolution and −123 dBm sensitivity for making demanding measurements on site or on the bench.

Tek 492 portability and rackmountability mean Dassault technicians can easily carry the 492 onto aircraft and conveniently test the signal quality of high performance radar, navigation systems and avionics. They measure signal amplitudes, distortion and spectral purity at millimeter wave frequencies and at 20 MHz IF. Amplitude resolution in superfine 0.25 dB steps provides precise measurement of signal differences, and the 492 is ruggedized to meet the same MIL-spec required of equipment being tested.

Additionally, the 492 helps make EMI measurements between on-board systems and devices to be installed in the aircraft. It enables technicians to assess at a glance emission levels over a wide range of frequencies.

Tek 492 digital storage provides consistently sharp, flicker free displays, plus functions such as SAVE A, B MINUS SAVE A, MAX HOLD and noise averaging, with which to compare, subtract, save maximum values, and smooth spectral displays. "An exceptional convenience," Mr. Geller says.

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"This kind of operational ease is most essential in isolated field locations," Mr. Geller says, "and an important time-saver in the lab."

Service. Calibration. Control. All in a day's work.

In-lab applications include equipment calibration, troubleshooting, repair, and testing new equipment upon receipt to ensure it meets the manufacturer's published specifications. These are more ways in which Electronique Serge Dassault achieves the maximum value possible from its 492 Spectrum Analyzers.

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High performance plus portability means capability unmatched at any price. If your measurements are confined to LF through UHF bands, the Tek 496 can meet your needs with additional savings. It comes standard with digital storage and phase-lock stabilization. Programmable versions of the 492 and 496 add their own outstanding benefits as GPIB instruments.

Contact your nearest Tektronix Field Office (listed in major city directories) for more information. Or in the US, call 1-800-547-1512 for descriptive literature. (In Oregon, call 1-800-452-1877).

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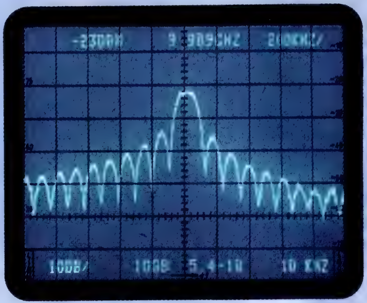

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Circle 134 on reader service card

which is below the end-of-life voltage of two 1.5-V batteries. The maximum output current is 100 mA (the load impedance should be 16 Ω). The output noise voltage is 140 μV for the BTL configuration or 100 μV for stereo. The voltage gain is fixed at either 32 dB (BTL) or 26 dB (stereo).

The TDA7050T is encapsulated in an eight-pin SO-8 package, which makes it suitable for surface-mounted assembly or for use in thick- and thin-film hybrid circuits. Samples are available now; prices depend on the importing country.

Philips, Elcoma Division, Building BA, 5600
MD Eindhoven, the Netherlands
[Circle 442]

Bubble-memory units offer 256-K- or 512-K-byte capacities

In the offing from Plessey Microsystems is the PBU85E, a microprocessor-controlled nonvolatile bubble memory with capacities of 256- or 512-K bytes. The PBU85E has a serial interface that emulates Digital Equipment Corp.'s TU58 tape systems. The unit is programmable to most serial data protocols. It has an access time of 36 ms to the start of any 512-byte block of data and a transmission rate that can be varied from 38.4 to 75 kb/s.

A boxed system with the form factor of a half-height 5¼-in. floppy-disk drive, the PBU85E is designed to give system builders an alternative to short-lived embedded tape systems that need regular maintenance. Without routine maintenance, the bubble memory's mean time between failure is higher than 50,000 h, and its maker says product life exceeds 10 years. It uses a 5-V dc supply and consumes a maximum of 3 A when the memory is being accessed and only 0.5 A when it is standing by.

In evaluation lots, the 512-K-byte version costs £1,950; its 256-K-byte counterpart £1,394. In production volumes, they are expected to sell for £990 and £750, respectively.

Plessey Microsystems Ltd., Water Lane,
Towcester, Northamptonshire NN12 7JN,
England [Circle 444]

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Basic Specifications of Multi-Color Liquid Crystal Display Modules

Item / Model	Number of Pixels	Total Number of Dots	Display Area (mm)	Outside Dimensions (L × W × T, mm)	Display Color	Back Light
FT1616	160 × 64	480 × 64	105.6 × 42.2	170 × 100 × 20max.	8colors (Blue, Green, Red, Black, Cyan, Purple, Yellow, White)	Fluorescent Lamp
● FB2416	240 × 64	480 × 64	158 × 42	230 × 100 × 20max.	4colors (Green, Red, Black, Yellow)	Fluorescent Lamp
● FT2416	240 × 64	720 × 64	158 × 42	230 × 100 × 20max.	8colors (Blue, Green, Red, Black, Cyan, Purple, Yellow, White)	Fluorescent Lamp

● **FB2416** and **FT2416** will be available soon.

* Specifications subject to change without notice.

Basic Specifications of Dot Matrix Liquid Crystal Display Modules

Item / Model	Outside Dimensions (L × W × T, mm)	Viewing Area (mm)	Number of Display Characters	Character Size (mm)	Power Supply Voltage	Interface Format
M3212	186 × 32.8 × 9.4	147.4 × 16	32 Characters × 2 Lines	2.9 × 4.1	5.0, −5.0 *	Parallel
M3214	210 × 80 × 12.1	152 × 40	32 Characters × 4 Lines	3.50 × 5.15	6.5	Serial
M4012	186 × 32.8 × 9.4	147.4 × 16	40 Characters × 2 Lines	2.65 × 3.75	5.0, −5.0 *	Parallel
F1632	210 × 80 × 12.1	152 × 40	Full Dots	Full Dots	6.5	Serial
F2416	220 × 80 × 12.7	160 × 53	Full Dots	Full Dots	5.0 * *	—
F4816	270 × 70 × 12.7	225 × 44	Full Dots	Full Dots	5.0 * *	—
F481C	290 × 110 × 12.9	225 × 74	Full Dots	Full Dots	5.0 * *	—

* Typical Voltage of V_{LC} is -1.5V. * * Built-in temperature compensation circuit.

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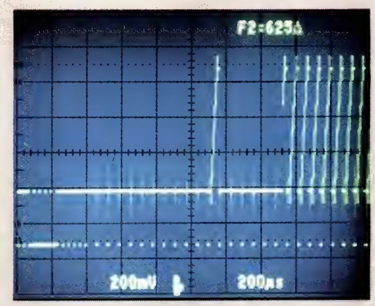

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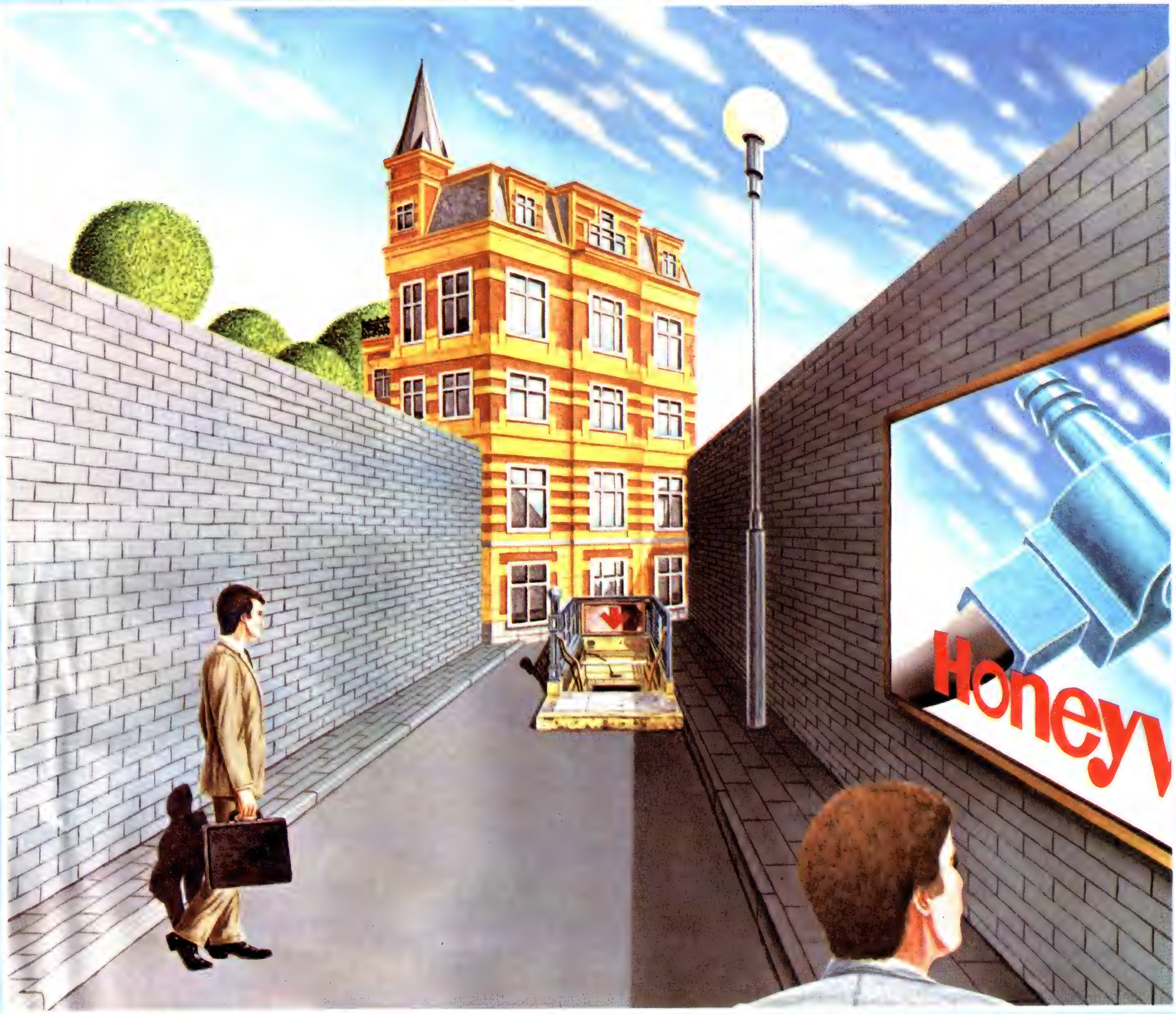

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Inside the news

Analysis of technology and business developments

Nationwide paging to use fm subcarriers

Beeper industry faces some pitfalls in setting up wide networking, but many operators are jumping into the market as deregulation hits

by Terry Feldt, Communications Editor

Thanks to the Federal Communications Commission's deregulation drive, coast-to-coast paging services seem set to burgeon. Among the FCC's actions to open up the airwaves to the market [*Electronics*, March 22, p. 89] is a freeing-up of unused spectrum in fm broadcast channels. What's more, an FCC action in April has even preempted individual states from restricting the market entry of new players.

Nonbroadcast services such as paging were taboo on fm until last year. But deregulation opened the door to low-cost piggybacking on existing transmitters, and paging-service operators are moving aboard. Nearly 2.5 million paging receivers are beeping now, but nationwide paging entrepreneurs such as Reach Inc., Lincoln, Neb., hope that the numbers might spurt over 1,000% by 1990.

Dollars and sense. The money aspects of adding SCA capability to a local fm transmitter have been right all along. SCA stands for subsidiary communications authorization, a bureaucratic term the industry has adopted to describe fm subcarriers.

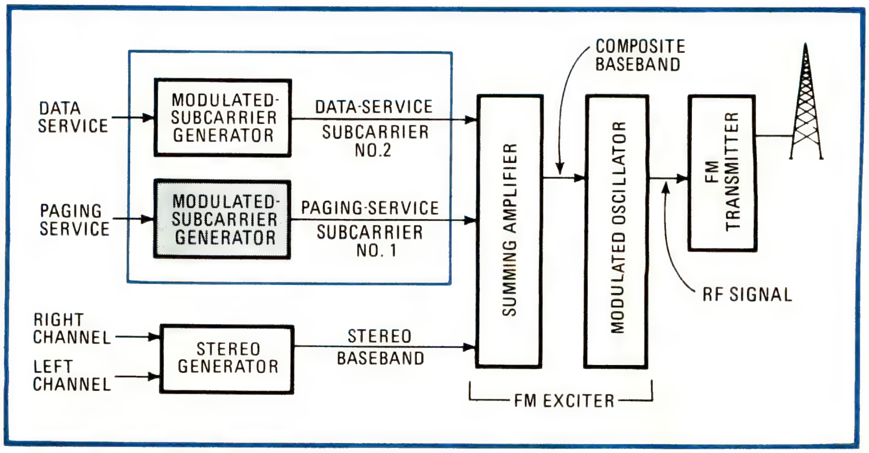
"With current technology, a modern station can add SCA capability for about $500 to $2,500 per subcarrier," says John Lyles, manager of fm engineering operations at Broadcast Electronics Inc., a Quincy, Ill., equipment manufacturer. Most is spent for an SCA generator (see figure). Such an expense is dwarfed by what it might cost to put up a conventional radio-paging transmitter, not to mention the inevitable bureaucratic delays encountered when entering a spectrum that is still, for the most part, tightly regulated.

Now, there are many more subcarriers up for grabs. In April 1983, the FCC moved to eliminate the 75-to-100-kilohertz guard band and thereby cleared the path for more than one subcarrier per station (or, as another option, an SCA with 46 kHz of bandwidth) with little restriction on modulation.

At the same time, the FCC virtually deregulated SCA usage, opening the door to such nonbroadcast applications as paging. In late March of this year, the SCA community was further buoyed by an FCC ruling that permits station owners to increase the frequency deviation when a subcarrier is in use. The higher frequency deviation is a boon to SCA operators, who have occasionally had trouble persuading station owners that the 1 decibel of signal-to-noise degradation resulting from the activation of a subcarrier was unlikely to hurt a station's market share.

Although station owners can now rest at ease about their signal strength, SCA operators, who shortly will have conventional paging interests to compete with for the nationwide business (see panel), still have to worry about the reliability of fm-subcarrier penetration in dense metropolitan areas—areas which hold the most lucrative market for paging. The designers of the new SCA networks, however, mindful that any paging system conceivable may experience outages as users operate from metal-framed buildings, are turning to technology to keep their beepers beeping everywhere.

Minimizing errors. American Diversified Capital Corp., Costa Mesa, Calif., for example, plans to use error-correcting codes and message repetition, as well as ferrite rather than wire-loop antennas, to lessen the chances that one of its Diversicom pagers might miss a page. According to Bob Switzer, project manager and director of marketing for



Exciting. Besides feeding an fm transmitter with a stream of pages, more generators can be added to carry new subsidiary communications services—even one-way nonbroadcast applications—such as dispatching trucks or sending out financial data to bank branches.

the planned nationwide network, "the pager not only scans and selects the proper radio station, but it also alarms when [a] signal is unavailable for utilization." Switzer hopes to have the top markets covered within 18 to 24 months after the first fm subcarrier goes active in June.

So far, slightly more than 50 fm stations have signed up with American Diversified. The firm will send its pages by satellite to each Diversicom station office, which in turn will feed at least one key transmitter in each market. Peripheral fm station capacity will be leased on an as-needed basis to augment coverage in very dense areas.

As the number of subscribers grows, the network will selectively address pages to one or more markets. As blueprinted now, however, the system—sending all pages nationwide—can support 160,000 users, who will be charged $20.50 per month per pager for the service, Switzer says.

To conserve spectrum, the system will support only digital paging—early pagers will have a numeric display for the return-call phone number; later units will sport alphanumeric readouts. The double-sideband-modulated paging signal will sit on a 57-kHz subcarrier, and American Diversified plans to make money with the bulk of the SCA capacity—leased but not needed for narrowband digital paging—by piggybacking other data services such as utility load management.

States thwarted. Already the fair-haired boys of deregulation, SCA operators received another shot in the arm in April, when the FCC preempted state regulatory agencies from hampering SCA entry into local communications-services markets. Lynette Green, director of affiliate sales for Reach, which operates a paging system called Spantel, says that this latest FCC order "removes one of the final obstacles to getting stations into the system."

Reach hopes that Spantel will evolve into a national network for tone paging and messaging. Having signed up over 100 affiliate operators since its inception in February 1983 (some 35 are now on the air), the firm expects to rely on up to 400 affiliates as it goes nationwide.

In Spantel, affiliates are currently tied into the network through landlines, but a switchover to satellite links is planned when traffic patterns are established. Wide-area service—at 92 kHz from all affiliate transmitters—is billed at a base rate of $5 (plus service usage) per pager per month. Local affiliates determine their own subcarrier frequency and the charges for local paging.

The newest models of frequency-agile pagers will provide an in-range and out-of-range indicator so that users will at least be aware if they have stepped into a "hole." Tone-only and digital-display paging services are planned: the Spantel system currently supports only tone and voice pagers.

Green contends that the entry of new paging services into markets in which conventional radio common carriers were operating had been difficult in roughly 60% of the states. They were demanding assurances that a proposed activity would serve an unmet public need. But with the FCC's deregulation of subcarrier usage and its hands-off directive to the local bureaucrats, the SCA crowd is positioned to enter virtually any market that is already serviced by an fm transmitter.

Free enterprise. Of course, fm stations are proliferating, a situation that makes established radio common carriers increasingly uneasy about the potential competition from all this unregulated SCA capacity. For instance, for paging operations at Cal Autofone, a Eureka, Calif., radio common carrier that services 700 pagers, president June E. Smith claims, "We spent almost $10,000 this year on legal work and engineering studies due to regulations at the state and federal level."

Complete deregulation of SCA, frets Smith, "can very adversely affect businesses in small market areas. Without states regulating SCA entry, ensuring quality service at reasonable prices, people will be jumping in and out of the market. And it will give everyone in the business a bad name."

Avid competition for three new channels

The Federal Communications Commission has assigned three frequencies just below 932 megahertz for nationwide paging, and the competition to use them is intense—16 hopefuls have applied. Unlike the new services using fm-subcarrier technology (known as SCA, for subsidiary communications authorization), these operators are banking on the tried and true technique for radio paging: a dedicated ultra-high frequency and multiple transmitters to fill in any holes that a single transmitter cannot reach. Current rumblings are that the FCC will hold a lottery to select the three winners, but applicants who consider themselves the fittest—those now beeping to a significant number of pagers in local markets—do not like this approach. For them, the stakes in this new game are too high.

Paging operators see big opportunities for integrating their existing facilities with a nationwide network because, "once you're on the road, a local paging service is basically useless," says Whitey Bluestein of MCI Airsignal Inc., Washington, D. C. MCI has thrown in with other radio common carriers—Metromedia Inc., Secaucus, N. J., and Communications Industries Inc., Dallas—in a bid to win a nationwide frequency. The three operators together have placed about a half million local pagers in the street—giving them a quarter of the total market, estimates Bluestein. He is general manager for the joint enterprise, called National Message Network, in which American Express Co., New York, is the fourth partner.

The joint venture would send out its pages to local transmitters on a packet-switched data network overlaid on the existing wide-area network run by another MCI subsidiary, MCI Telecommunications Corp. Still, like most national SCA networks, every transmitter in the country will not generally broadcast every page. "It is not efficient at all to broadcast a page nationwide. So you really have to aim a little," says Bluestein. **–Terry Feldt**

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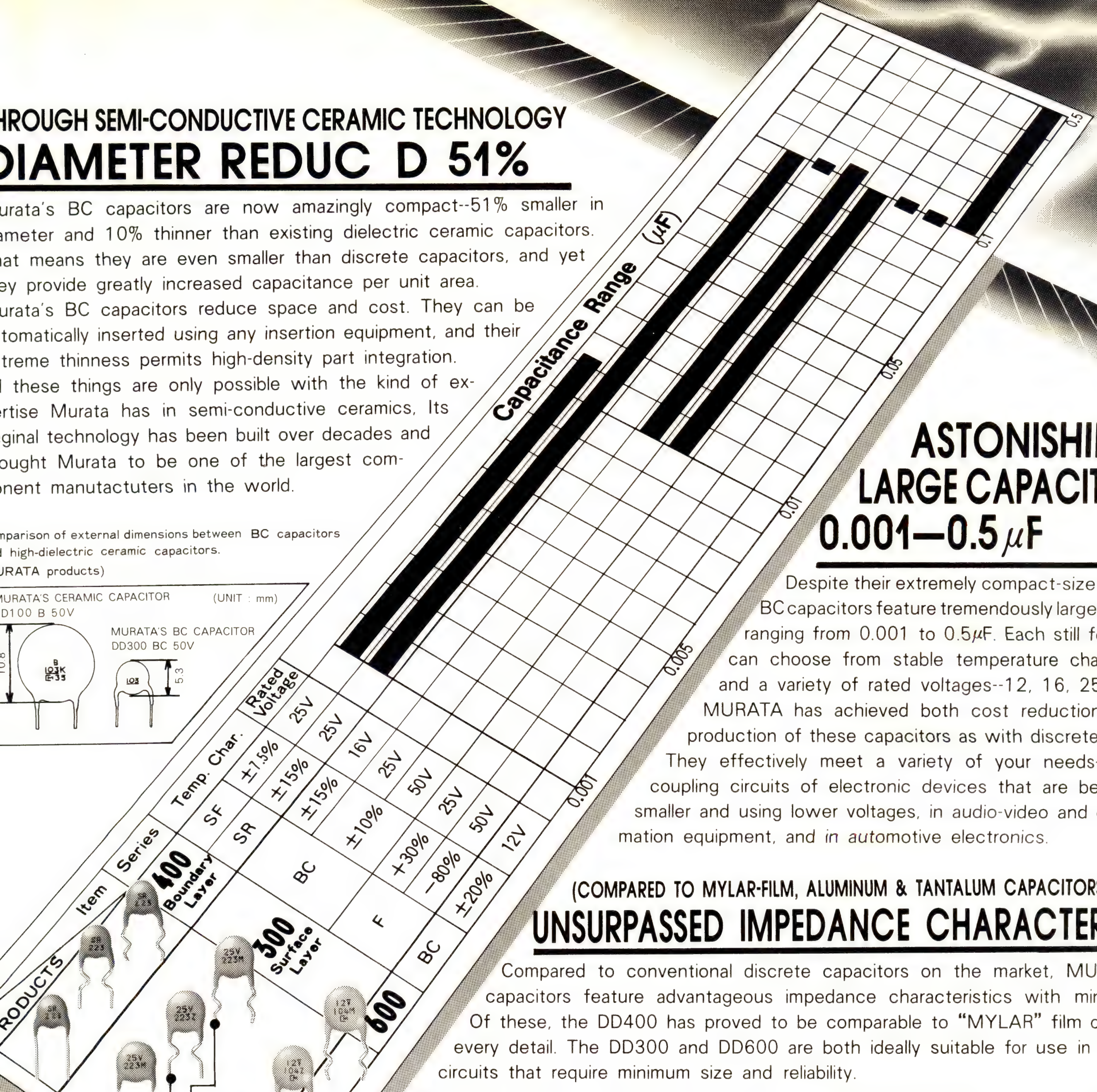

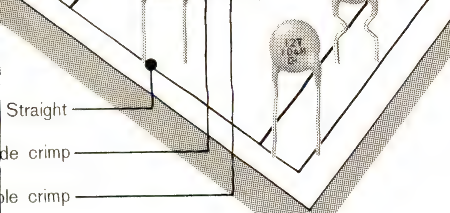

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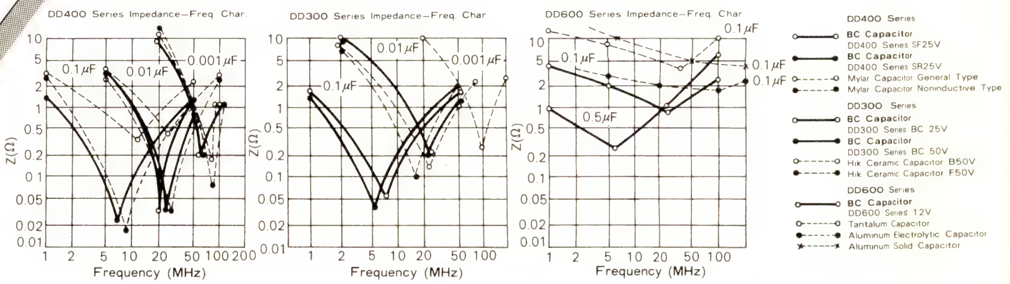

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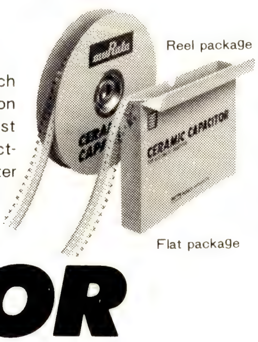

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Systems integration

Closing in on open systems

With lower tiers of the seven-layer interconnection model standarized, a worldwide push is well underway to develop the high-level protocols

by Robert Rosenberg, Systems Integration Editor

Ordinarily, the National Computer Conference is a sort of 20th Century Tower of Babel, with a myriad of languages making communications between information-processing systems difficult if not impossible. But at July's NCC in Las Vegas, hardware from 14 major companies will be linked in two landmark demonstrations that show how far along the world's computer makers are with open-systems-interconnection (OSI) standards and what remains to be worked out before off-the-shelf hardware from different producers can be readily melded into a system.

One of the demonstrations will be an industrial network for factory computers, based on a token-ring local network developed by General Motors Corp., New York. The other, a local net for offices worked out by Boeing Computer Services Co., a division of the Seattle, Wash., plane maker, uses a scheme for collision-sensing multiple access with collision detection. For both nets, the National Bureau of Standards played a key role, setting up network testing and measurement standards.

The list of companies involved in the two demonstrations ranges from giants such as International Business Machines Corp., Digital Equipment Corp., and Hewlett-Packard Co. to much smaller firms such as Advanced Computer Communications, Charles River Data Systems Inc., and Concord Data Systems Inc. Behind these players is an international supporting cast of hundreds of people working out the protocols and standards that are the driving force behind open-systems architecture.

Their work already has culminated in well-defined standards through the first five layers of the OSI model. The flashy full-color videotex graphics moving from screen to screen under control of file-transfer protocols on the Boeing local net or the models of manufacturing processes used on shop floors driven by message-handling protocols on the General Motors net will prove that. With the first five layers in hand, the drive is on around the world to finish the job on the top two layers (see figure).

High stakes. Getting there will be half the fun—or more. Because of the huge markets at stake in open-systems architecture, there will be much jockeying behind the scenes as the standards get hammered out in organizations such as the International Organization for Standardization, which originated the OSI model, the Consultative Committee on International Telephony and Telegraphy, the European Computer Manufacturers' Association, and the American National Standards Institute.

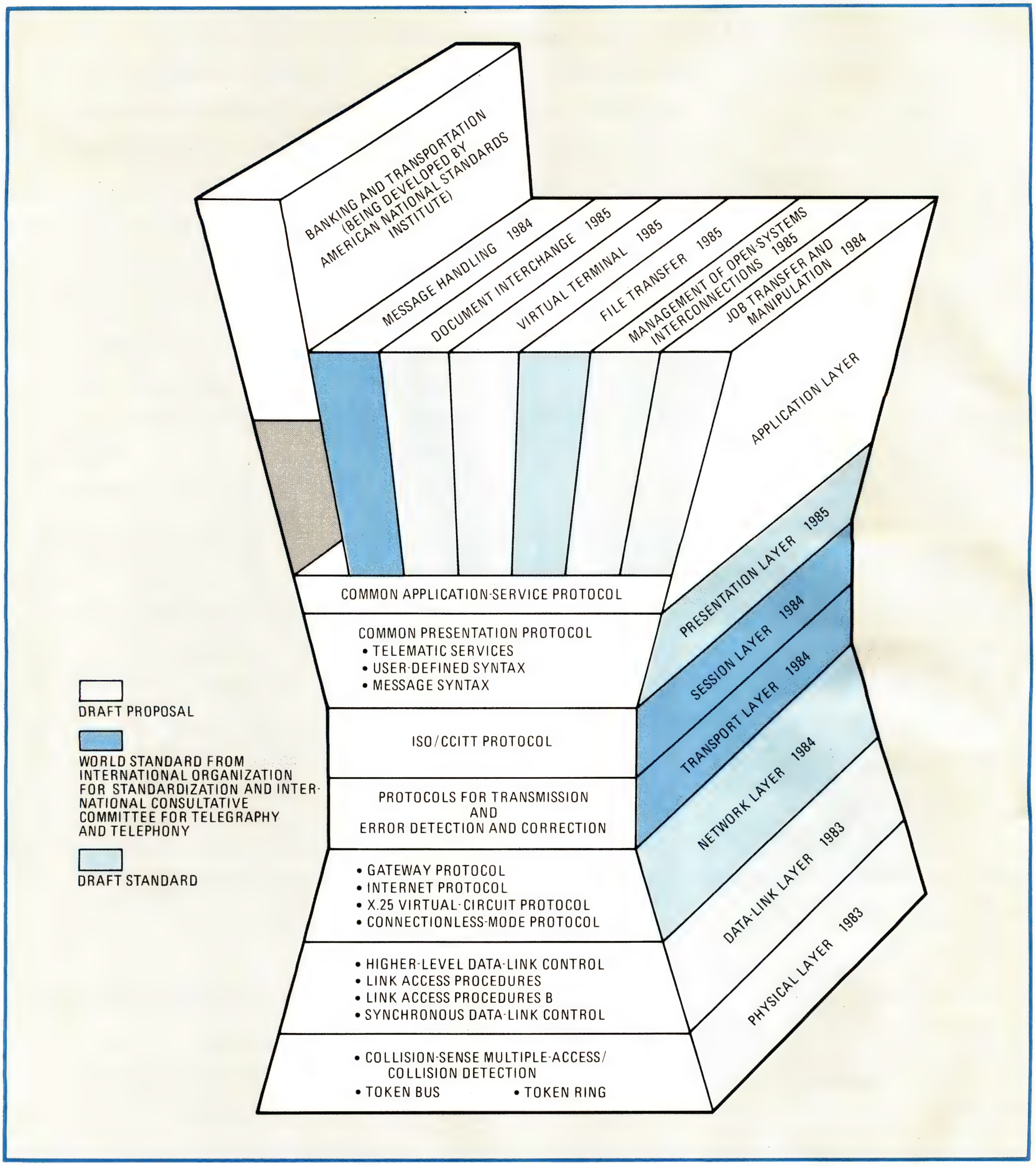
Actual figures do not exist, but an idea of the enormous market involved in making heterogenous machines talk to one another comes from projections for local nets, which are only one segment of it. Kenneth G. Bosomworth, president of International Resources Development Inc., a Norwalk, Conn., market-research firm, estimates that local-net sales this year, excluding terminals and work stations, will run at $110 million. They will increase to $400 to $500 million by the end of the decade as per-node connection costs plummet to 25% of today's price. In Europe, the market is expected to vault from $32 million in 1983 to $145 million in 1988, while component prices drop at least 30% a year, according to market researchers Frost & Sullivan Inc., New York.

Bosomworth points out that the larger U. S. manufacturers, with a full spectrum of products, find themselves in a double bind: "Anything that provides complete open connection allows [someone's] customer to become someone else's customer." On the other hand, he allows, "Most companies would welcome some level of standardization" to facilitate product planning.

If U. S. manufacturers are of two minds on what advantages open-systems architecture will have for them, European manufacturers are not. Recently, when 12 of them announced their intention to implement OSI standards—among them France's Bull, Italy's Olivetti, the UK's Plessey and ICL, West Germany's Siemens, and the Netherlands' Philips—some observers interpreted the move [*Electronics*, March 22, p. 63] as the opening gambit in a European counter-offensive against increasing U. S. and Japanese marketing pressures.

Japan, too, is developing a concerted strategy. Nippon Telegraph & Telephone Public Corp. began developing the Japanese Data Communication Network Architecture in 1977—well before OSI—and it is promising to have a full-blown, all-digital, integrated network blanketing the country by the year 2000. Meanwhile, a nationwide university net is already operating (see "Higher protocols for higher education in Japan," p. 81).

The NTT effort appears well on its way after a six-year research effort involving 300 persons. Both lower- and higher-level protocols have already been implemented, says Tsu-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APPLICATION LAYER
PRESENTATION LAYER 1985
SESSION LAYER 1984
TRANSPORT LAYER 1984
NETWORK LAYER 1984
DATA-LINK LAYER 1983
PHYSICAL LAYER 1983
COMMON APPLICATION-SERVICE PROTOCOL
COMMON PRESENTATION PROTOCOL
• TELEMATIC SERVICES
• USER-DEFINED SYNTAX
• MESSAGE SYNTAX
ISO/CCITT PROTOCOL
PROTOCOLS FOR TRANSMISSION AND ERROR DETECTION AND CORRECTION
• GATEWAY PROTOCOL
• INTERNET PROTOCOL
• X.25 VIRTUAL-CIRCUIT PROTOCOL
• CONNECTIONLESS-MODE PROTOCOL
• HIGHER-LEVEL DATA-LINK CONTROL
• LINK ACCESS PROCEDURES
• LINK ACCESS PROCEDURES B
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Open system. ISO's open-systems-interconnection model is wide at the base and the top, where many standards exist. The narrow middle has only a few compatible standards.

kasa Kawaoka, chief of NTT's Data Communication Network Section, Yokosuka. The lower levels of DCNA all conform to OSI, while the upper levels can readily be adapted to OSI once the standards are firmed up.

The European firms, however, are not simply responding to the threat to their home markets by the Japanese or IBM. Their cooperation began over two decades ago and stems from the political milieu of the early 1960s, which engendered several European cooperative ventures, notably the European Economic Community. Since its founding then, ECMA, headquartered in Geneva, has been aggressively driving standardization work.

ECMA's strategy, if one can believe U. S. standards makers, is to push through a "quick and dirty" standard in a hurry and then let ISO pick it up for refinement. "I don't think they speed us up," says the chairman of an international standardization committee, who requested anonymity. "But if they do, hallelujah."

ISO, based in Geneva, develops

standards for everything from screw threads to solar energy, but the key group in it as far as OSI goes is subcommittee 16 of Technical Committee 97, which sets the agenda for information systems. So well has the subcommittee done its job of developing protocols for peer-to-peer communications between computers that proponents of hierarchical approaches—notably International Business Machines Corp.—want to break it up.

The other major player involved in establishing international standards is CCITT—a part of the Geneva-based International Telecommunications Union. ISO is a member and so has a say in CCITT's decisions, which pertain mainly to international regulations that are set for government-dominated postal and telecommunications services.

Yankee views. Among the trade associations of the U. S.—where prevailing wisdom usually favors the marketplace as the ideal forum for standards to emerge—support for the OSI varies from cautious optimism to outright enthusiasm. The acceptance of the standardization effort among hardware and software suppliers is generally high, but, muses an official of one trade association, "OSI, it seems to me, has a wonderful generality about it."

Still, some confusion exists as to which layers and options should be built into a particular product line, leading one engineering manager of a local-network manufacturer to complain, "I don't think there is much of a requirement for a CAD/CAM system to communicate with the automated teller machine down the street."

The Electronic Industries Association, however, which operates out of Washington, D. C., already uses the OSI model in many of its numerical-control standards produced for industrial applications. The EIA views the OSI as attractive because of its flexibility—the model can be adjusted to the future technological changes. But drawbacks are evident. "The OSI is a complicated model. As time goes on, one would hope that it will become more simplified. That's what usually happens in standardization," notes Jack Kinn, EIA staff vice president of engineering.

The OSI express is also the vehicle of choice for the Computer and Business Equipment Manufacturers Association, based in Washington. Says senior director Bill Hanrahan, "All of our members are of a firm belief that the development of standards based on the OSI reference model is the necessary way to go."

Family scene. To outsiders, the behind-the-scenes maneuvering of companies, national groups, and international standards organizations looks to be highly contentious. But disputes are more family squabbles than clashes between clans. By and large, the standards makers respect each others' technical competence.

Alain Bourguignon, who heads the networking and communications department at Bull, the Paris-based, government-controlled computer manufacturer, points out that one of the most important factors behind the realization of international standards for data-processing networks is the agreement between ISO and CCITT to work together toward a common standard when they are interested in same subject. "The ISO brings together the normalization organizations of all countries, and the CCITT , the telecommunications agencies, while ECMA is an association of manufacturers with absolutely no legal power," Bourguignon explains.

As an example, he singles out the protocol for the OSI transport layer. It operates on the data blocks that the network layer transfers to and from the lower layers, associating them with virtual-message channels. The protocol was originally defined by ECMA as its standard No. 72, then converted by ISO into its 8072/8073, and finally classified by CCITT as its X.214/.224.

The next level up the ladder is also transport-oriented. Called the session layer, it is used to initialize, run, and terminate transactions.

Now ISO is close to approving draft standards for the transport and session layers that are word-for-word compatible with the CCITT documents. The approval could come this fall, says John Neumann of Ultimate Corp., Santa Ana, Calif., head of the cognizant committee (ANSI X3T5.6) of ANSI, which represents the U. S. in ISO. "I suspect there will be few changes that will cause the two versions [the CCITT and ISO documents] to diverge," he says.

Ready for bed. The NBS's Robert Blanc shows off the test bed that will qualify gear from nine firms for a multisupplier local network scheduled to be demonstrated at this summer's NCC.

The protocols of the next higher level—the presentation layer—interpret the syntax, or character representations and data formats, of the information that is to be communicated between peer OSI systems. In this case, both CCITT and ISO have proceeded in step toward the approval of the documents, according to Paul D. Bartoli, who is the international standards planning group supervisor for AT&T Information Systems as well as vice chairman of the ANSI X3T5.5 committee on presentation and application layers. Both the session service definition and the session protocol documents have been drafted, but they have not been submitted for confirmation as draft proposals. That could happen as early as next month, however, meaning that a draft standard should come out in 1985.

ISO and CCITT also are cooperating closely to work up a common descriptive language for generating protocols. Beginning in the early 1980s, the two groups independently recognized the need. CCITT had formalized its work in the Specification and Description Language, while ISO worked to develop two languages. These two languages had enough features in common with SDL that they cross-fertilized the common language now evolving.

Post haste. The whole alphabet soup of standards-making bodies is scurrying to finish up the protocols for OSI's top layer, which covers specific applications. One that is well along is electronic mail. CCITT began work on a standard for storing and forwarding messages—which was regarded as a logical extension of teleprinter services—and it has blossomed with facsimile, graphics, and voice messaging.

Eight documents today make up the X.400 series of working recommendations for message handling, and they will likely become draft international recommendations (which is CCITT's diplomatic phrasing for standards) at the organization's plenary session in October. CCITT and ISO versions for message handling are very similar, but Ian Cunningham, of Bell-Northern Research in Ottawa, Canada, chairman of the responsible CCITT study group, expects the standards will be tweaked "to meet the additional needs of ISO."

The NBS will presumably support only the basic portions of the message-handling protocols, leaving details to be thrashed out in the marketplace. When it announces that decision, NBS will also define the limits of Federal standardization in message handling, says James R. Moulton, a staff expert following OSI developments at NBS's Systems and Network Architecture division, in Gaithersburg, Md. He thinks that decisions about other areas in the X.400 protocols are best left to manufacturers (for the British position, see "UK government promotes open-systems model," p. 82).

Many have made their decisions already and put electronic-mail products on the markets around the world. ITT Dialcom Inc., Silver Springs, Md., for example, is licensing its electronic-mail software under such names as Minerva in Australia, Telecomm Gold in the UK, and Telebox in Germany. General Electric Information Services Co., Rockville, Md., is negotiating with overseas postal and telecommunications agencies to license its Quik-Comm electronic-mailbox services. TymeNet Inc., San Jose, Calif., is also providing OnTyme electronic-mail services.

Passing documents throughout a system is a more complex task than person-to-person communication of messages, since for documents the communication is between machines. The protocols involved reflect the increased sophistication of office automation, which requires capabilities such as translation between fonts and type sizes and integration of photographs and black-and-white line drawings. All these refinements, of course, must be carried out in a manner transparent to the user.

ISO has subdivided the task of developing documents standards into five working groups that roughly mirror the structure of a document (see "Standards for the automated office," p. 83). Two of these groups—one for text structures and one for text preparation and presentation—have ended their skirmish on the boundary between what the elements of text are and how those elements get processed. They reached an accord in mid-May at a meeting in Berlin. At that meeting, the ISO text structures group was ordered to rework its overview document to align it with developments in CCITT. The document defines three major elements in text preparation:

- The office-document architecture, which describes the rules for compatible handling of a page's elements by different machines.
- The document profile, which will act as a preamble to documents and provide such information fields as security classification of the document, author, date of issue, and other data.
- The office-document interchange format, which may adopt the X.409 syntax developed by CCITT for message handling.

According to Roy Pierce of Xerox Corp., Austin, Texas, who heads the ANSI text-structures committee, "We are very pro [X.409] and very strong for its usage. I think it is in good standing" in the international standards community. Meanwhile, still another of the five groups, the one that is working on text inter-

Higher protocols for higher education in Japan

The only network with fully functional higher protocols in Japan is the Inter-University Network, or N-1, which links 40 campuses across the island nation. The network comprises seven host computers at the major national universities and 33 satellite computers.

Because it was begun before the open-systems-interconnection standardization work started, the N-1 system is not compatible with OSI, says Tadao Saito, an associate professor of electrical engineering at the University of Tokyo. "We had to consider compatibility with IBM and its compatible-mainframe competition, Fujitsu and Hitachi, in designing this architecture," he explains. N-1's high- level protocols include remote job entry and a virtual-terminal definition. The net also provides for generation of Japanese characters using ASCII codes.

Because of all the varying protocols now in use, Saito thinks it is virtually impossible to achieve standardization: "The only way to enforce *real* standardization in our market is for one manufacturer to dominate." Also, he sees two major impediments in Japan. "First, if the Ministry of Posts and Telecommunications takes too strong a hand in setting domestic standards, they open themselves to foreign complaints that they are creating new trade barriers. Second, the computer makers nonetheless want at least some guidelines, which could help them lower development costs." **–Michael Berger** change, is on the verge of divulging its draft proposal.

Another crucial OSI application is a set of standards for virtual terminals so that users can be certain that what goes in at one end will be what comes out at the other. Because all the important control characters and functions—such as paper advance and carriage return—have been implemented in a variety of ways by manufacturers, ISO is developing an interface protocol for functions. Virtual terminals then will come in a variety of flavors as manufacturers pick and chose those features most appropriate to their markets.

ECMA has been working in the virtual-terminal area for several years. The Europeans first thought that the biggest markets would be in the machines that are appropriate for airline reservation systems and in those that use a fill-in-the-blank menu-driven system. Seeing a larger potential elsewhere, however, they have since shifted their interests to developing graphics terminals and to terminal management, which is the ability to switch modes or classes of services, much as windows do in microcomputers.

As a result of a compromise struck with ANSI, ECMA has taken the lead in the terminal-management and graphics areas. Other parts of the agreement are that both the ECMA half-duplex and the ANSI full-duplex communications schemes would be part of any ISO standard, and that ANSI's definitions for terminating a terminal interaction would be adopted by the Europeans.

Definitions for the basic class of terminals are "pretty well sorted out, [and] ECMA is fairly happy with it," says Henry Lowe of Digital Equipment Corp., Maynard, Mass., a representative on both the ANSI and ISO committees.

Crossings. Protocols to manipulate and move files among systems are perhaps further along than any other of the applications layers. The OSI file-service protocols define transfer, access (or manipulation), and management by developing a common model of a file called the virtual file store and then using this common descriptive model to enable otherwise incompatible filing systems to communicate.

By defining common file attributes and a common structure and operation, the virtual file store provides the generalized landscape needed to construct local mapping functions to smooth the differences between systems. The pertinent draft international standard should be forthcoming in 1985.

But more work remains, according to those working on the standard. "We've placed the hooks appropriately for access management," says Douglas Lewan, of AT&T Information Systems, Lincroft, N. J., and a member of the U. S. delegation to the ISO virtual-terminal working group. But, he adds, a much richer management structure is needed so that records can be accessed and manipulated efficiently.

In fact, management functions in OSI are generally still nascent, but they are needed to control peer-to-peer application processes as well as the total OSI environment. For example, protocols must be developed so that two open systems can pass resource-allocation information, access-control information, security, and bookkeeping data.

According to Don Sheppard of the Canadian Imperial Bank of Commerce, in Toronto, and chairman of his country's advisory committee on OSI , "What's been done is [to complete] the most obvious requirements" for management while waiting for some of the application-processes areas to reach greater maturity

Work on JTM. Job transfer and manipulation (JTM) protocols, necessary for doing tasks such as searching a data base in Tokyo from a terminal in New York, will come later. Hal Foltz, who is executive director of Omnicom Information Services Inc., a Vienna, Va., firm specializing in tracking OSI developments, says that the JTM group will probably have a working version ready for consideration as a draft proposal at some point this summer.

As the application layer matures, industries that have heavy information requirements will develop OSI-compatible standards. For example, ISO has more than 12 well-established standards developed by the banking industry, but these are not yet tuned for OSI. The ANSI X9 banking group wants ISO to make sure that any upcoming standards are compatible with existing national financial networks.

The U. S. transportation and credit industries, under the auspices of ANSI committee X12, are developing standards for purchase orders, invoices, payment and remittance, and other protocols needed to conduct and process business transactions. Edward Guilbert, president of the Transportation Data Coordinating Committee, Washington, D. C.,

UK promotes open-systems model

In a bid to catapult small manufacturers into the huge markets that the open-systems-interconnection standards should bring and at the same time counter the de facto standards set by the large multinational computer makers, the UK government has come up with its Intercept strategy. The brainchild of the Department of Trade and Industry, Intercept is intended to identify and promote the more mature OSI standards in order to help relatively small manufacturers pin down shares of the burgeoning open-systems market.

K. A. Bartlett, the head of Information Technology Standards at DTI and an authority on the OSI standards, concedes that they "are absolutely essential to the industry," but maintains that "the sheer scale of the exercise is daunting and the overlap between [the standards organizations] is causing difficulties." To give manufacturers a guide to navigate the standardization maze and quicken the acceptance cycle, the Intercept program is going to track the development of potential OSI standards. Besides "recommending" certain budding OSI standards, DTI is going to provide tutorial material, seminars, and test facilities. Grants to develop products using Intercept recommendations are also being discussed.

–Robert Rosenberg

X12 work, says complete agreement between European and U. S. trade associations is still in the future, but he expects that it can be reached.

Getting international agreement on videotex standards has proven difficult, according to all accounts. Having just bundled videotex, facsimile, document-interchange, and a number of other graphics-oriented services together under the rubric of telematic services, CCITT therefore has agreed to three international standards: the North American Presentation Level Protocol Syntax (NAPLPS), Europe's Conférence Européenne des Postes et Télécommuncations (CEPT) scheme, and finally Japan's Character and Pattern Telephone Acess Information Network (Captain).

Roy Bright, the chief executive officer of Intelmatique, the international marketing arm of the French telecommunications agency in Paris, explains that the three protocols are a consequence of different methods to keep the cost of character-generation down. The Europeans, the first to make commercial use of the technology, developed an inexpensive decoding system based on alpha-mosaic primitives to decrease the requirements for expensive local memory. By the time the Canadians began evaluations, memory costs plummeted, making higher-quality bit-mapped graphics possible, and potential advertisers—never a prominant factor in the European market controlled by state-governed PTT monopolies—clamored for the higher-cost technology, said Bright.

The several hundred characters that make up the Japanese kanji alphabet dictated a third approach. "Very large sums, already exceeding $250 million, have been invested in the States" Bright says, and the stakes are going to increase since "any application that has an interest in the mass consumer market" is fair game for videotex.

Proprietary nets. As might be expected, IBM dominates when it comes to proprietary networks. The firm has installed its layered Systems Network Architecture all around the world since it was introduced in 1974. Much like the later OSI concept, any SNA system can talk to any other SNA system. For compatibility between OSI and SNA , two approaches have been discussed: OSI might be implemented in the individual SNA product itself, or a protocol conversion could be performed between the SNA and OSI domains.

Like IBM, Xerox has a proprietary offering, Xerox Network Systems. But unlike IBM, Xerox makes no bones about plans for bringing its product into line with OSI. According to Jerry Elkind, vice president for systems integration at Xerox Systems Group, in Palo Alto, Calif., "the intention is to bring our network into conformance" with ISO's open architecture.

He says that older products will probably be retrofitted with gateways and newer products designed for compatibility. But he cautions that standardization has "got to go beyond printing [a specification]; it is necessary but not sufficient"—a lesson Xerox learned when the Ethernet parameters were tweaked so much by some manufacturers that compatibility problems arose.

At the NEC Corp., in Kawasaki, Naoshi Shima, an executive at the company's business-marketing and product-planning department, says work is underway on its Distributed Information-Processing Network Architecture. He said that DINA conforms with the official Japanese Industry Standards, and since the government decided two years ago to make JIS compatible with ISO standards, NEC is striving for full OSI compatibility. Inevitably, however, JIS is a superset because of the special problems of kanji generation.

Shima says the argument is still going on internationally over standardization at higher levels, though "if ISO decided on such standards tomorrow, we would support them—but such standards are just a dream right now." There are two paths to follow, IBM or the market, he continues. "We are following the market, trying to develop as many end-user-need products as possible.

"We see the small-computer and minicomputer market in Japan growing at an annual rate of 20% to 30% in the next decade," he says, "and we have a 60% to 70% share of that market, so we are developing DINA products applicable to both large- and small-computer markets in Japan."

Toshiro Kawamura, a software engineering manager at NEC, reports that the firm has been using a sophisticated job application in an integrated office and factory automated system at a factory in Abiko, near Tokyo. Other research includes development of voice-and-image architecture; the main body of work is finished, and an experimental implementation is underway, he says. ☐

Standards for the automated office

Automated offices must handle heavy traffic in electronic documents having both text and graphics, so the International Organization for Standardization has set up a subcommittee in its hierarchy of standards-writing committees to develop standards for preparing and transmitting them. The work has been split up among five groups:

- The user requirements group is querying users to find out what needs to be standardized and passing that information along to the other four groups.
- The terms and symbols group makes sure that the nomenclature conforms to ISO parlance.
- The text structures group is developing a description of documents, based on two basic characteristics: the logical structure (elements such as chapters, paragraphs, footnotes, and the like) and the layout structure, which defines the set of rules necessary to create the logical structure.
- The text interchange group is deciding the transfer syntax—that is, how the document is moved across the network.
- The text preparation and presentation group is defining the functions necessary to manipulate the elements of text to reassemble them on an output device such as a printer or video terminal. –**Robert Rosenberg**

Additonal reporting for this article was provided by Michael Berger, Tokyo; Terry Feldt, Communications and Microwave Editor; Robert T. Gallagher, Paris; John Gosch, Frankfurt; and Kevin Smith, London.

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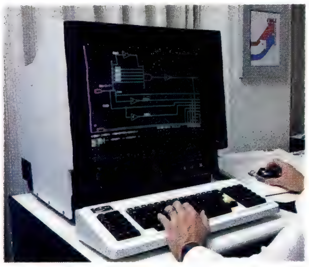

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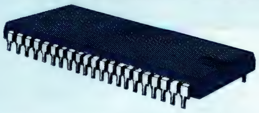
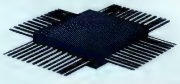
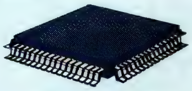
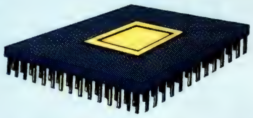
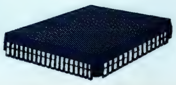
	720	48	NOW
	1440	66	NOW
	2000	84	NOW
	4205	120	NOW
2 μm / 2ns	6000	140	1985
	8000	160	1985
	10000	172	NOW
	20000	200	1985

PACKAGING TYPE		PINS	AVAILABILITY
DIP		16-48	NOW
PLASTIC FLAT		32-88 132	NOW 1985
CERAMIC FLAT		60	NOW
PIN GRID ARRAY		72-176 240	NOW 1986
PLASTIC LEADED CHIP CARRIER (PLCC)		18-84 132-176	1985 1986

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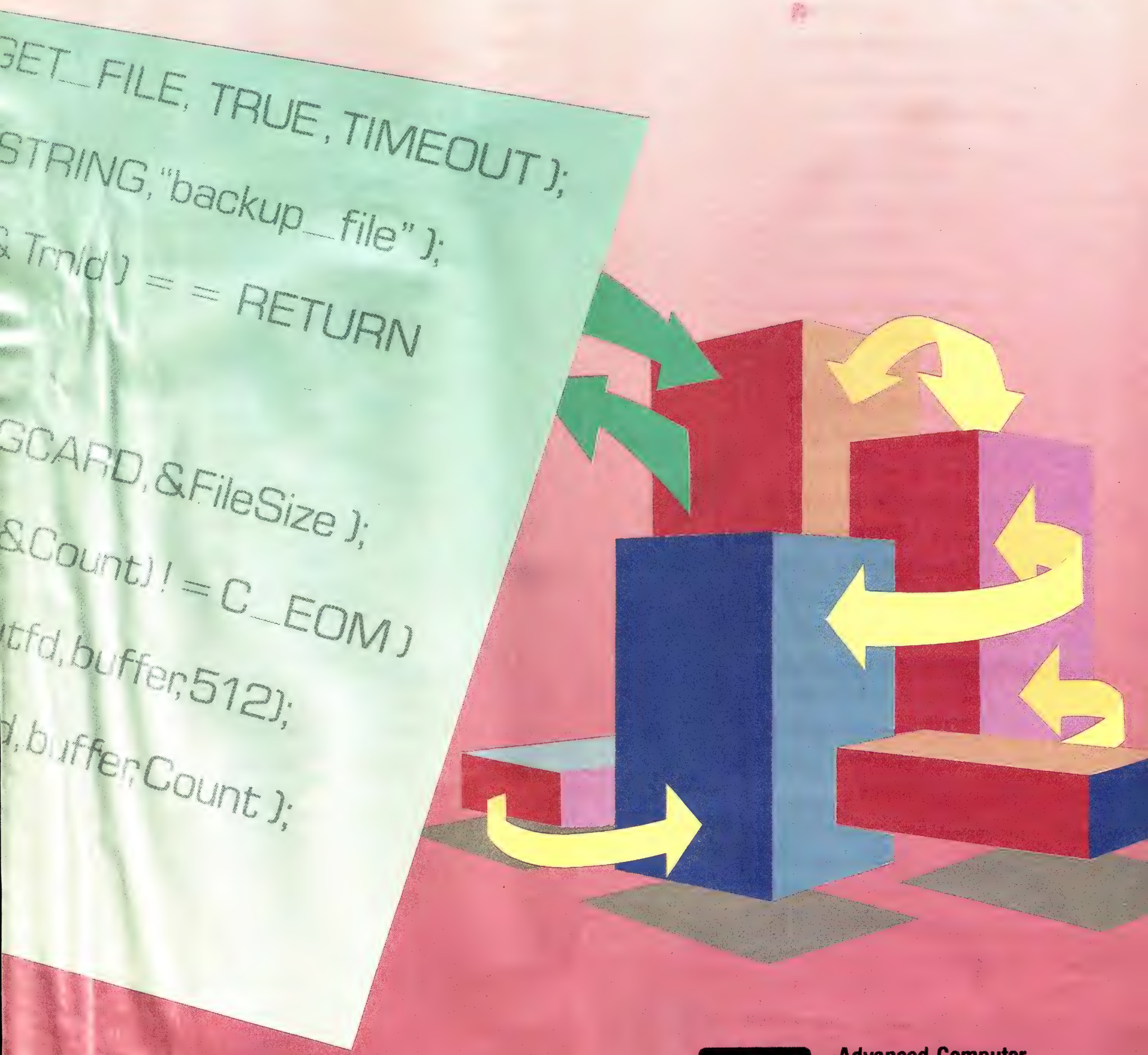

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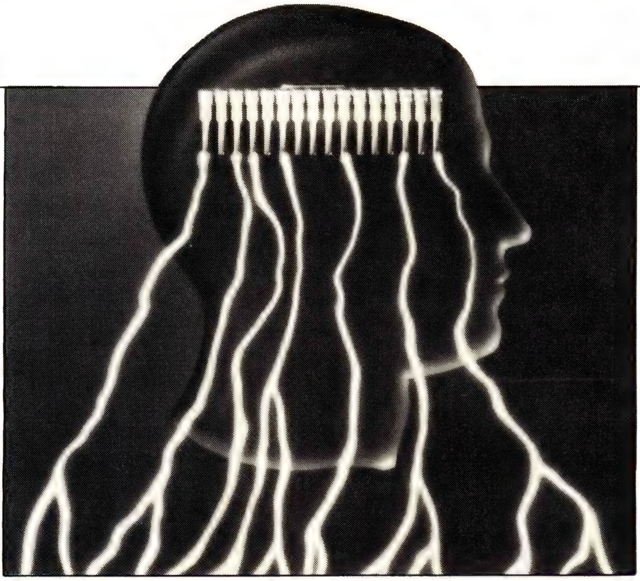
Smart-power technology ushers in era of logic and power on a single chip



by Ashok K. Bindra, *Components Editor*

☐ Until recently, both bipolar and MOS power devices were used in discrete form and controlled by external circuitry. Now, however, advances in both technologies have helped researchers merge logic, control, and power on the same chip and thereby produce an integrated circuit called a smart power device. As these new and versatile components continue to gain acceptance, they are revolutionizing circuit and system designs, primarily by simplifying them. These ICs are touted for use in switching power supplies, protection circuits, and motor drives; indeed, they are finding applications that range from telecommunications to home appliances. This may well be one of this decade's most exciting areas for semiconductor development.

The merger of logic and power on a single chip represents a combination of brain and brawn. Not only does it mean more efficient power switching in telecommunications equipment and household appliances, but it also clears the way for the eventual microcontrol of power distribution for all applications. Nonetheless, the art of integrating high-power circuitry and logic on the same chip is in its infancy. Still, smart ICs have been reported with many configurations and technologies: bipolar, MOS, or a combination of the two.

Art Fury, vice president of marketing at Siliconix Inc., a Santa Clara, Calif., pioneer in power MOS field-effect transistors, says that the expanded capabilities of smart power ICs should encourage the development of totally new products that previously were not possible or practical. Just as the microprocessor chip, only a few years back, stimulated new thinking that ultimately created many new products, so too smart power ICs will inevitably create new applications and opportunities. Fury expects the device to revolutionize the design of many electrical products, including high-efficiency variable-speed induction motors, induction heating systems, high-frequency power controls, and power-line buses.

At Motorola Inc.'s Semiconductor Products Sector, in Phoenix, Ariz., smart-power technology—known as Smartpower—combines a high-power bipolar output transistor and a small-signal complementary-MOS control circuit. The pnp power device is vertical, with the collector on the back of the die, permitting higher current control for similar die sizes. Currents higher than 25 amperes have been controlled with die sizes of less than 200 square mils. These smart power ICs can dissipate 250 watts and control switched loads of more than 2 kilowatts, with the breakdown voltage of the output power device generally exceeding 100 volts. By combining such vertical power structures with planar IC technology—which provides control, interface, and protection functions—Motorola has produced a number of cost-effective smart power chips.

Motorola's MPC100 series of linear voltage regulators is one example; capable of dissipating 80 W, it can regulate currents up to 10 A. A cross-section of one of these regulators (Fig. 1) illustrates the variety of active devices the monolithic structure can integrate. The chip includes bipolar pnp and npn transistors, as well as n- and p-channel FETs. The pnp device forms the vertical-output power transistor and serves as the substrate upon which the control circuitry is fabricated. Top metalization connects these devices in order to form the final circuit. Now the technology's capabilities have been expanded to include other power devices, such as power npn transis-

Varying configurations of high-power devices, low-voltage logic control, and protection circuits are revolutionizing applications and IC designs

tors, T-MOS (so named because the drain current splits in a T formation) power FETs, and power T-MOS silicon controlled rectifiers, and is known as Smartpower II. In fact, it is now possible to use this technology to construct almost every active device commonly used in circuit designs.

Good protection

The integration of T-MOS SCRs with C-MOS control logic is well suited to protection circuits, and Motorola's MPC2005—an overvoltage- and temperature-protector IC—takes full advantage of this technology. It protects sensitive electronics from overvoltage transients and extreme temperature environments: it senses the fault condition, which occurs when the trip-point voltage (6.3 V) or temperature (125°C) is exceeded, and quickly crowbars, or short-circuits, the supply.

Besides improving on traditional techniques to increase performance and reliability, the integration of T-MOS SCRs with monolithic-control circuitry substantially reduces chip size, complexity, weight, and cost. The T-MOS SCR guarantees immunity to high voltage changes over time, high current-handling capability, extremely fast turn-on times, and accurate control of delay times from the onset of overvoltage detection.

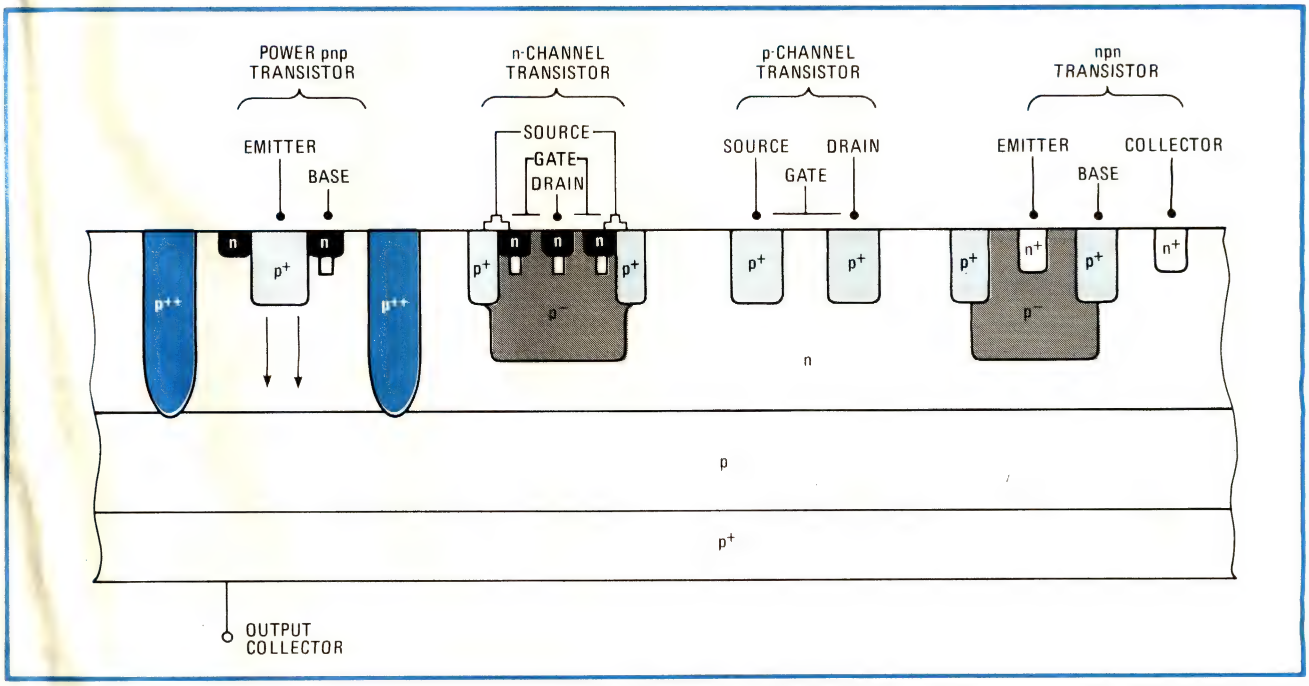
Like monolithic voltage regulators, overvoltage-protection ICs generally use a bandgap circuit to establish the voltage reference. Given this reference, little additional circuitry is required to turn an overvoltage-protection IC into an overtemperature-protection IC as well (Fig. 2), because the same bandgap circuit that establishes a voltage reference also has well-defined temperature characteristics. Temperature measurement is performed with the aid of a comparator. Since the overtemperature circuitry takes up less than 2% of the total die area, the two functions are combined at very little cost. The trip-point temperature is set to monitor the chip's heat-sink temperature. Since the internal power dissipation of this part is only milliwatts, its die temperature equals that of its heat sink. If the chip is mounted in free air, the monitoring temperature is equal to the equipment's ambient temperature.

A third terminal, for optional use, is also provided—a connection that performs voltage-trip-point and delay-time adjustments, remote sensing, and remote triggering. This last application allows the overvoltage protector to be used as a smart SCR. The comparator input, with its 2.4-V threshold and high impedance, is well suited to direct drives from a variety of logic circuits. Placing this protection device in proximity to the load or on a printed-circuit board eliminates interference resulting from physical separation. The result is increased safety and improved reliability.

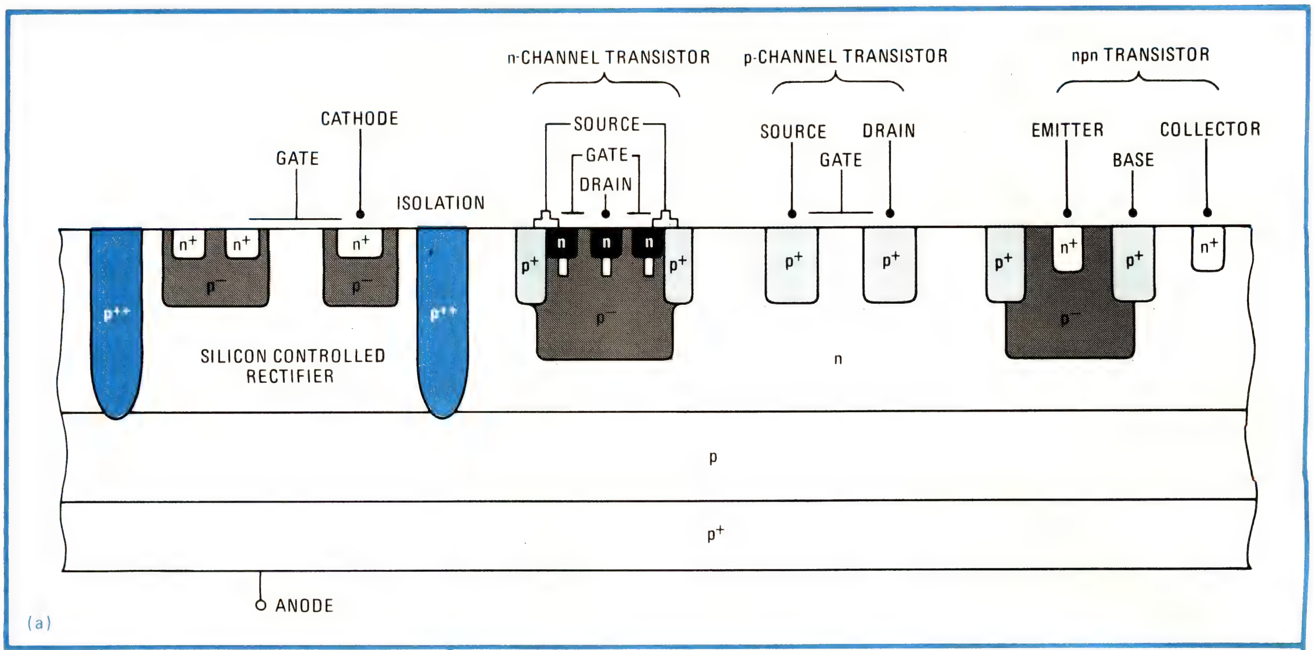
Smart-power switch

A slight modification of the overvoltage protector's cross-section results in a T-MOS-FET output. This modified output device is an n-channel FET implemented in Motorola's XPC1500 logic-to-power switch, designed to switch power loads of up to 16 A on commands received from C-MOS logic or TTL inputs. The company plans to introduce this smart power device sometime during the third quarter of this year.

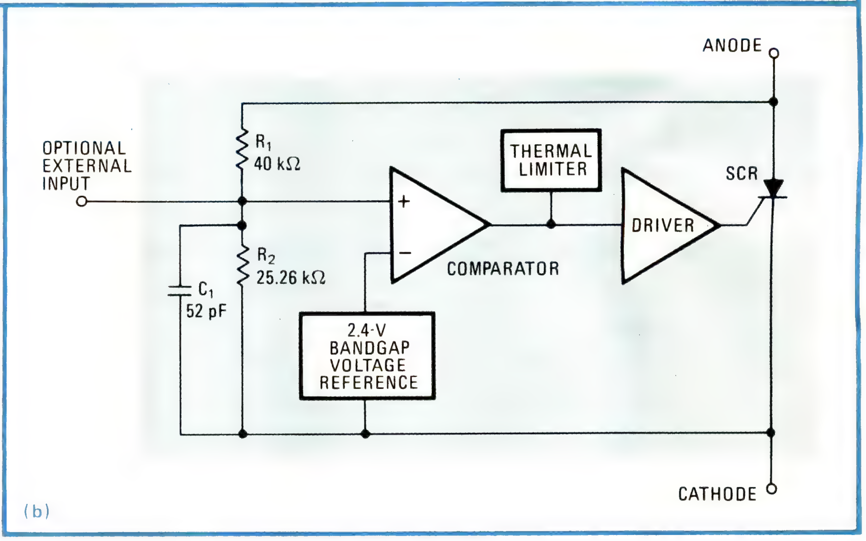
Additional features include almost zero drive power during the on state and optional breakdown voltage for the power FET, controlled turn-on and turn-off times,



1. Mixed process. In Motorola's Smartpower MPC100, the high-power pnp transistor is integrated along with C-MOS and bipolar transistors on a single chip. This monolithic smart linear voltage regulator can dissipate 80 watts and regulate 10 amperes.



2. Smart protector. A T-MOS SCR (so named for the T formation of its drain current) is the high-power output device and is integrated with C-MOS logic (a) in Motorola's MPC2005, a smart-power overvoltage-protection circuit. A third terminal (b) is available.



inductive spike control, and direct connection to the positive supply rail. In addition, using a power FET as the output device makes it possible to control loads of different sizes by just changing the T-MOS FET's size during the layout stage, with little or no change in the C-MOS control circuitry. Further, because the switch's on voltage is low and the switching speeds are the same as those of power FETs, power dissipation is minimal and system efficiency is correspondingly high.

Another smart power chip under development at Motorola is the XPC1600 pulse-width-modulation power circuit, which is designed for switching-regulator and motor-control applications. Its integral-power MOS FET can withstand 150 V at a maximum drain current of 10 A.

The greatly reduced gate-drive requirements of the power MOS FETs make them ideal candidates for the output devices of smart power ICs. International Rectifier Corp., in El Segundo, Calif., is using this application with its photovoltaic relays. Here, a light-emitting diode illuminates a pile of photovoltaic cells, whose output transforms the LED's light directly into electrical energy. This output, though small, is sufficient to trigger the gate of a MOS-FET output switch that can control up to 1,000 V. It includes a bidirectional MOS FET called BOS FET (for bidirectional output-switch FET) and control logic on the same chip, which is then linked to a photovoltaic pile illuminated by the LED. Lateral double-diffusion-MOS transistors with voltage-breakdown capabilities higher than 1,000 V were used to fabricate this common-gate, bidirectional-output-switch FET.

The integration is achieved because each of the BOS FET's two drains and the control circuitry has been placed in its own n-well. The high-resistivity p-type substrate provides high voltages without increasing the on-resistance usually expected in power MOS devices. Also, a careful combination of diffusions eliminates the parasitics that would otherwise be caused by the proximity of high-voltage high-power output devices to low-level control circuitry. Last, careful layout eliminates the latchup between terminals.

Another smart power device from International Rectifier, one that is capable of switching several hundred watts and introduced well before the photovoltaic relay, is the S^3X (for solid-state switch with zero crossing) solid-state relay. This power chip includes an optical receiver, a signal conditioner, a zero-crossing detector, and a high-power thyristor [*Electronics,* Dec. 29, 1982, p. 59]. Bipolar has been combined with C-MOS technology, thus reducing the component count to only three semiconductor chips: two ICs and one LED for optical isolation. One of four conduction levels interconnects all three chips on a common substrate. The first is a diffused interconnection, the fourth a thick aluminum conductor for handling the power output. The middle two levels are isolated polysilicon conductors.

Optical isolation is difficult with the monolithic approach and thermal management, and the conflict of incompatible technologies is a major obstacle, too. International Rectifier has therefore decided to take the hybrid route. As long as size and thermal management are under control, the company sees no reason to abandon its commitment to hybrid solutions.

Multiplexing analog signals

Supertex Inc., in Sunnyvale, Calif., is another semiconductor manufacturer that is dedicated to making smart power MOS FETs. The company implements its HV10 family of analog multiplexers with a combination of silicon-gate C-MOS and D-MOS on a monolithic chip. Each member of this family can be partitioned into four functional blocks: input protection and buffers, a C-MOS logic array, control-voltage level shifters, and high-voltage D-MOS output bilateral switches.

The low-voltage logic section is made in an n^- epitaxial tub using a p^- well technology, while input protection to both ground and positive supply is handled by diffused-current-limiting resistors and diode protection; guard rings prevent latch-up. A unique dual-gate p-channel FET shifts the level of the gate-drive signals from those of C-MOS to the positive and negative high-voltage rails. This FET comprises two separate transistors stacked one atop the other, with a common diffusion as the source of the bottom FET and the drain of the top one. When the gates of each transistor are properly biased, the blocking voltage is shared equally between them.

If made with the conventional *thin* gate oxide, the FETs would have had a breakdown voltage of no more than 100 V. By using a thick gate dielectric—greater than 1 micrometer—the surface electric fields are reduced and breakdowns higher than 200 V achieved.

The large-output n-channel transistors have a lateral D-MOS structure, and each output device resides in its own n^- epitaxial tub, isolated from the rest of the circuit by the p^+ isolation diffusion. In addition, placing an n^+ buried layer at the epitaxial-substrate interface below each output transistor minimizes the substrate current flowing through the parasitic bipolar transistor, formed by the p^- body, n^- epitaxial layer, and p^- substrate. The buried layer reduces the parasitic pnp's current gain to less than 0.1, thus keeping the substrate current to a minimum. Merging low-voltage logic with high voltage and high current on a single chip produces high-perfor-

Great-shape controversy

For a given on-resistance in power MOS field-effect transistors, the question has been raised about which cell pattern is best for small dies: triangular, square, rectangular, hexagonal, circular, or parallel-line structures. To date, most MOS-FET makers agree on only one thing: that clearer answers are likely to take shape in the next five years as chip geometries become finer and intelligent-power integration becomes greater. Meanwhile, nearly a dozen manufacturers are even now touting their own choices as the best candidates for the cell shape.

So far, theoretical expectations in wafer fabrication have not yielded conclusive results, says Raymond T. Ford, manager of power-MOS products at RCA Corp. in Mountain Top, Pa. Early expectations were that the right cell shape would allow companies to increase the active areas of chips and to cut on-resistance. But Ford and many of his industry colleagues now believe that the anticipated second- and third-order effects of cell shapes have not yet had a major impact on the ability to do either. Currently, most think the greatest improvements can be achieved by improved processing, packaging, new designs in chip periphery, and the like. RCA, like International Rectifier, General Electric, and Unitrode, is using hexagonal cells, which it regards as less susceptible to uneven electrical fields at high voltages thanks to the polygon's lack of very sharp corners.

A rare start-up in the power market—Texet Corp. of Allen, Texas [*Electronics*, June 30, 1983, p. 53]—has a new triangular cell, optimized for lower-power MOS FETs (below 200 volts). The firm believes it can have a significant impact on the cost of power MOS FETs with its Trimos technology, forcing established competitors to reconsider the significance of cell shapes for packaging densities under 200 V. Meanwhile, Texet plans to use square cells on devices above 200 V. It says it is now working on a 1,000-V discrete chip for introduction later this year.

In the square-cell camp are such major manufacturers as Motorola, Siemens, and Siliconix. Besides square cells, Siliconix Inc., of Santa Clara, Calif., is also using nonclosed, interdigitated cells for its metal-gate MOS FETs and some silicon-gate chips, which are designed for lower capacitance. Supertex Inc., in Sunnyvale, Calif., is producing MOS FETs with interdigitated structures, which it believes provide the lowest capacitance and ease interfacing to low-power logic. The square cell is also the favorite in Japan, where Toshiba, Matsushita Electronics, NEC, and Hitachi are all using it for their power MOS FETs.

Other cell structures such as parallel and serpentine lines as well as an experimental "basket-weave" configuration have been considered. Yet another approach is to lay out gate and source structures next to each other in patterns of interdigitated lines.

As new photolithography equipment makes finer line mance analog switches that help designers to improve system performance and reliability at lower cost than discrete solutions.

Besides multiplexers, Supertex is also offering a range of smart drivers for electroluminescent display panels. Its recently announced 64-channel row and column drivers, HV03 and HV04, complement this combination of D-MOS and C-MOS. As these panels move into color, a higher drive-voltage capability and greater logic density will be needed. Looking toward the display industry's future needs, the firm plans to increase the logic density from the present 2,000 gates a chip to 5,000, with voltage-handling capabilities of more than 500 V.

Texas Instruments Inc., Dallas, uses a bid-FET process—a merger of high-speed bipolar control circuitry, C-MOS logic, and high-voltage D-MOS transistors on a junction-isolated wafer—to produce an array of high-voltage drivers for display applications. TI has also found this technology to be well suited to the telecommunications market.

Combining processes

The development of smart power devices with low-voltage C-MOS control and high-voltage, high-current D-MOS outputs has produced three different ways of integrating C-MOS and D-MOS monolithically: self-isolated D/C-MOS IC technology, junction-isolated D/C-MOS, and junction-isolated D/C-MOS with complementary outputs (see the table). Although circuits fabricated with each of these processes are becoming commercially available, the economics of IC manufacturing and the design flexibility that junction-isolated D/C-MOS affords are combining to make this process more attractive.

Siliconix' first smart power-driver chip (Fig. 3), which contains silicon-gate C-MOS logic and junction-isolated D-MOS output transistors in a totem-pole configuration, has been fabricated with this technology. The input logic is TTL-compatible, with the low-voltage section operating from a 30-V supply, while the level shift is performed with high-voltage lateral D-MOS transistors. The two D-MOS output transistors are rated at 80 V, supplying 8 and 12 A, respectively. For sensing and controlling the current in each transistor, resistors are placed in series with the output transistors.

A major concern for designers of D/C-MOS circuits is the technology's performance in environments plagued by electrical noise. Though proper design can minimize the IC's sensitivity to latchup, that problem cannot be eliminated with junction-isolation techniques. Dielectric (as opposed to junction) isolation will certainly help here but also adds considerably to design costs.

Siliconix is considering another transitional approach using gate arrays instead of random logic in the smart section of the IC. The company says this technique is an attractive alternative to the standard power-transistor-plus-random-logic approach because it will cut costs, save time, speed production, allow small-volume preproduction runs, and provide the quickest and most efficient

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widths possible, many believe that cell shapes will play a greater role in lowering on-resistance, die area, and, eventually, costs. Also, some argue that higher voltages will bear out the advantages of cell shapes that do not have very sharp angles or concentrated electrical fields. Focused fields can produce a low breakdown voltage, which hampers off-state-blocking capabilities.

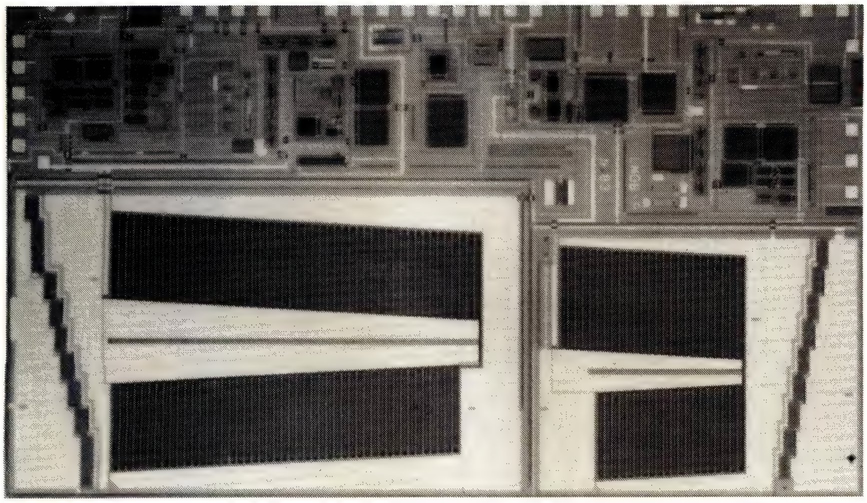
However, at low voltages, a triangular shape can now have a significant impact on the size and price of a chip, says Dorman C. Pitzer, device-development manager at Texet. By the summer, Texet plans to introduce its first discrete MOS FET based on Trimos. Jeff A. Hendy, marketing vice president, says that triangular cells will also be used later this year to minimize silicon area on Texet's first integrated power MOS-FET chips, now being designed for automotive applications.

To optimize Trimos for low-voltage applications, Texet is using right-angle triangular cells with 30-micrometer sides and a 42.42-μm hypotenuse. These shapes provide space savings of 15% to 17% compared with more conventional hexagonal or square cells, says Pitzer. Texet is also tailoring the polysilicon width separating each cell to further boost packing densities at given voltage levels. For example, polysilicon widths between cells on 60-V parts are 8.8 μm, while 600-V chips have spacings of 12 μm. With Trimos, Texet expects to utilize 88.3% of the volume of the dies, compared with about 85% utilization with other types of closed cells.

RTC-La Radiotechnique Compélec, the principal French subsidiary of Philips, chose an equilateral triangular structure for its MOS-FET technology. The firm believes that this geometry gives a more efficient use of silicon surface per square millimeter compared with hexagons or squares.

At International Rectifier Corp., El Segundo, Calif., hexagonal cells are being promoted as the natural choice. "You want to get the most perimeter for a given cell, and you want to get the best packing density. That problem was actually solved billions of years ago by honeybees," notes Derrick Lidow, vice president. The firm is using its Hexfet technology on several smart power chips. With today's processing equipment, hex-shaped cells represent a space saving of several percentage points over square cells. In the future, this small saving will become even more important to manufacturers, Lidow emphasizes.

Motorola Inc.'s power MOS-FET operation in Phoenix, Ariz., is enhancing its square-cell geometries by reducing the source width of its devices from 0.8 mil to 0.6 mil, says Jack Takesuye, product planner. In the long run, however, Motorola believes that MOS-FET packing densities and on-resistance can be optimized with parallel-line structures, once advances in photolithography equipment permit source widths to be cut to 0.4 mils. —**J. Robert Lineback**



3. Intelligent. This smart driver chip from Siliconix, fabricated with C-MOS and junction-isolated D-MOS technology, contains analog and digital control functions implemented using a silicon-gate C-MOS process and two large D-MOS output drive transistors.

commercial application of smart-power technology.

At first, Siliconix will be exploring the application of smart-power technology to commercial electrical products and military and aerospace systems. Currently, the firm is working with military customers, who have funded the project, to develop a smart power IC with enhanced capabilities at reduced cost.

Another player in the game is Texet Corp., a start-up in Allen, Texas. Throughout 1984, the company plans to introduce a series of smart power MOS FETs geared to the automobile industry and based on a new triangular gate architecture called Trimos. At first, the company plans to integrate a 30-V, 7-A power MOS FET with 800 gates on a single chip. It is also defining specifications for a smart power chip that will integrate D-MOS output devices with bipolar and C-MOS circuits. Of this chip, 60% will be devoted to the power function, 30% to the logic interface, and 10% to the control function, with the power-control section mixing C-MOS and bipolar technologies.

The merger of bipolar and C-MOS for smart power chips is not new to Sprague Electric Co., of North Adams, Mass. In fact, its UCN-4401A and UCN-4801A 4- and 8-bit latch and drivers, introduced several years ago, are examples of this art of integration. Since then, these simple ICs have evolved into sophisticated drivers for vacuum-fluorescent displays. For example, the UCN-5800 series of bi-MOS II devices has been designed for use as segment or digit drivers in high-voltage vacuum-fluorescent-display applications. Although the standard output rating is 60 V, a few selected parts have a maximum rating of 80 V and 40 milliamperes per driver. In addition, the new process allows greater density and vastly improved switching speeds. With a 5-V supply, a second-generation part will typically operate at better than 5 megahertz.

Junction isolation

Besides display drivers, the company is also making smart ICs for motor-drive applications, and it is now looking into ways of improving the more than 150-V breakdown capabilities of its bi-MOS chips. When this has been done, the company claims that the bi-MOS technology will be able to address plasma and electroluminescent-display-driver applications.

General Electric Co.'s research and development center in Schenectady, N. Y., has recently developed a bi-MOS process that allows the output devices to withstand 500 V. This 500-V junction-isolation process complements GE's recently introduced line of power MOS ICs. The high-voltage, high-power drivers made with this process can deliver up to 2 A peak, and can be used in a variety of applications including display drivers, switching power supplies, motor control, robotics, and automobiles.

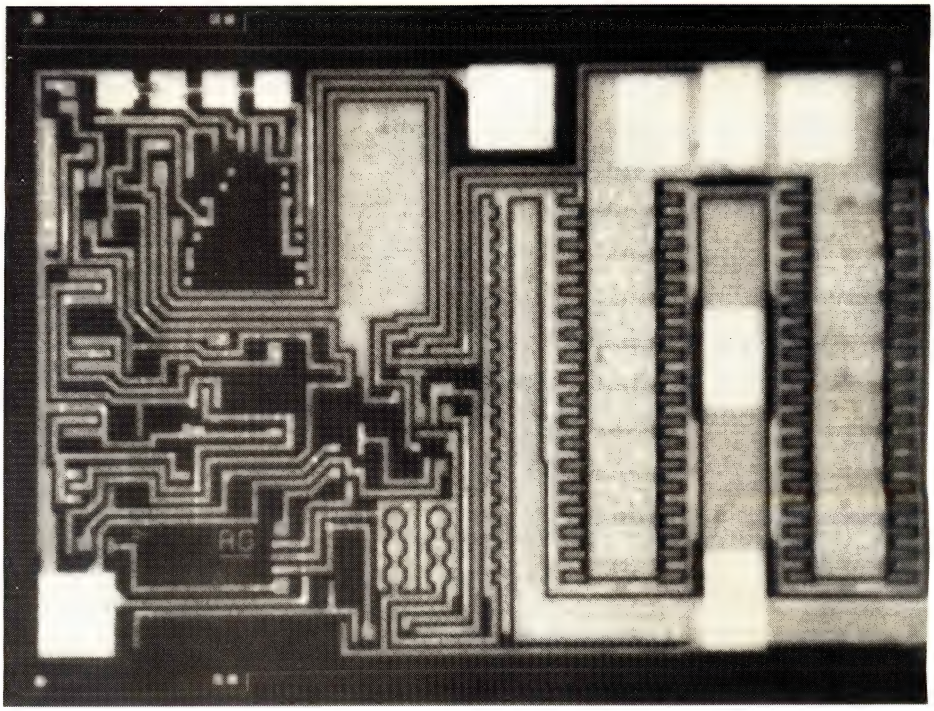
Harris Corp., Melbourne, Fla., introduced another example of smart-power technology—an induction-motor energy saver—at the 1984 PowerConversion International conference, in Atlantic City. Based on bipolar technology, the chip is a dielectrically isolated monolithic circuit with junction breakdowns of 400 V. Intended for use in single-phase induction motors, it can be operated directly from a 120/240-V ac line. Direct line connection is made possible by on-chip high-voltage regulators that generate a positive rail of

COMPARING FEATURES OF THE THREE DOUBLE-DIFFUSED C-MOS PROCESSES

Characteristic		Self-isolated process	Junction-isolated process	Junction-isolated process with complementary outputs
Fabrication	Epitaxial layer required	no	yes	yes
	Number of masking steps	9–11	10–12	11–13
Electrical	Logic voltage (V)	5–15	5–15	5–15
	Clock rate (MHz)	5	5	5
	Output voltage (V)	200–400	150	150
	Output configuration	single-ended (open collector)	single-ended, totem-pole	single-ended, totem-pole, push-pull
	Parallel resistance of output devices in 200-by-200-mil chip (Ω)	3–5	1–2	2–4
	Total on-chip current capability (A)	2–4	10–20	5–10

SOURCE: SILICONIX INC.

4. Control and power. Unitrode's UC7805 is implemented in bipolar technology and combines logic, control, and power circuitry. Capable of dissipating 20 W in a TO-3 package, the power devices occupy about 50% of this voltage-regulator chip, which requires no external components.



+35 V during the positive half cycles and a negative rail of –35 V during the negative half cycles. A high-voltage output stage converts the low-level signal from the comparators to a high-current switch that directly controls the gate of an external power triac.

Augmenting the smart-power arena with bipolar technology is Unitrode Integrated Circuits, of Merrimack, N. H., whose recently announced UC3717 is a bipolar monolithic chip for stepper-motor controls. The circuit comprises a low-power Schottky-TTL input, a current sensor, and an output stage with built-in Schottky protection diodes. Schottky diodes were preferred over their p-n junction counterparts because of their faster recovery times and lower forward-voltage drops, which cut electromagnetic interference and power dissipation in the chip. Also, the diodes provide thermal control by allowing the proper current distribution.

With established expertise in bipolar technology, Unitrode has fabricated smart power ICs to address a variety of applications. For example, the company's L295 dual-switch-mode solenoid driver is a monolithic IC suitable for such applications as hammer-driving in matrix printers, and stepper-motor driving. The UC7800 (Fig. 4) and UC7900 series of positive and negative voltage regulators supply current up to 1.5 A.

Taking the hybrid route

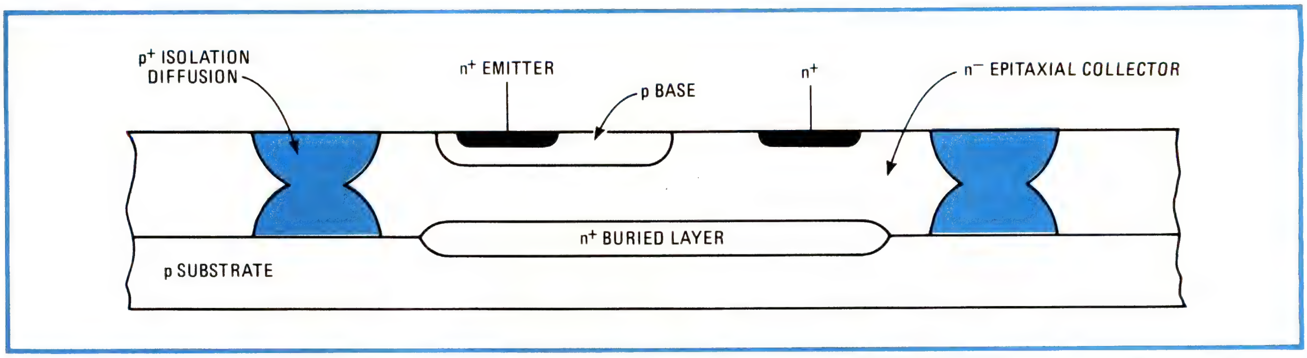
Although the present limit of Unitrode's bi-MOS technology is 5 A and 80 V, the company plans to enhance the capabilities of its smart power ICs by taking the hybrid route. Integrating a high-voltage, high-current discrete device with a control-and-logic chip in a hybrid package could in some instances be a better solution, says Bob Mammano, Unitrode's vice president of engineering. He adds that the monolithic approach requires too many trade-offs, and therefore is not always a cost-effective solution.

Early analysis of various smart-power processes has led engineers at National Semiconductor Corp. in Santa Clara, Calif., to conclude that in the near future, mixed processes will offer no real advantage over National's own low-dropout technology. This process is a modification and refinement of an earlier bipolar process called deep base, or double-diffused base. Pnp current-gain and breakdown voltage are among the features that are improved in the low-dropout process. Peak gain in a lateral pnp is usually a trade-off with the breakdown voltage.

With this fabrication technique, current gains in pnp transistors averaged more than 100, while breakdown voltages typically stayed at 80 V. In addition, field-plating techniques make breakdown limits of 120 V possible with no reduction in gain. And in some experimental devices, current gains greater than 400 have been obtained. National has used this modified process in its entire line of low-dropout regulators and plans to continue using it as the line is expanded.

U. S. semiconductor manufacturers have made tremendous progress in smart-power technology, but their most advanced overseas counterparts are tapping every resource to move ahead as well. Recent progress in bipolar-IC processing at SGS Semiconductor Corp., of Milan, Italy, has led to the introduction of new structures using ion implantation (Fig. 5), paving the way for the integration of high-voltage, high-current output stages with high-performance control sections. This new generation of smart power chips from SGS includes motor controllers, solenoid drivers, and switching power supplies.

The ion-implanted isolation technique, developed by SGS, overcomes two major hurdles facing the standard isolation process. The first problem is that standard isolation, formed by diffusing p^+ from above, diffuses in three dimensions and produces a semicircular cross-section. Consequently, a significant part of the transistor area is lost to isolation, which plays no active part in circuit operation. The second problem is the fact that standard isolation diffusion is a high-temperature process carried out after the collector-epitaxial growth.



5. Isolation. Progress in bipolar processes has led to the introduction of ion-implanted-isolation technology, in which the combination of high-voltage, high-power output stages with high-performance control sections becomes possible.

Subsequently, the n^+ buried layer spreads, reducing the n^- thickness between the base and the buried layer and therefore reducing the breakdown voltage.

The new process solves both problems by forming the isolation in two steps. The first is a heavy p^+ implant before the n^- collector-epitaxial growth, followed by a predeposition/drive-in from above. High-temperature processing is thus reduced to a minimum, which increases the breakdown voltage and reduces the area occupied by the isolation.

Such developments in IC technology have made it possible to integrate power transistors capable of delivering 50 V and 5 A on a monolithic IC with relatively complex control circuitry. SGS's L295 combines the power transistors and control circuitry for a current-controlled solenoid driver. Available in a multiwatt package, the chip contains the drive circuitry for two solenoids and can supply as much as 2.5 A to each of the loads. Additional features include an on-chip protection circuit that disables the chip when the junction temperature exceeds the maximum rating, a TTL-compatible input, and inductive load control.

Smart FETs and Mosbips

The L298, a monolithic dual-bridge driver for motor-control applications, is another smart power device from SGS. It can deliver up to 3 A peak in each bridge output, with independent enable inputs for each. Paralleling the two bridges increases the chip's power capability to 150 W. Configured as a pulse-width-modulated switching regulator is its cousin, the L296. This single-chip switching power supply includes the control circuitry needed to implement a pulse-width-modulated switching power supply, as well as circuits for current and thermal protection, overvoltage sensing, and soft start, and a 4-A power transistor for the output. To obtain high switching speeds, the output npn transistor is driven from a circuit that provides both turn-on and turn-off signals for the power stage.

Munich-based Siemens Corp. is also involved with smart devices, which the company calls smart FETs, for automotive applications. Employing MOS techniques, its microprocessor-controlled parts are intended as high-speed switches for inductive and resistive loads in automotive applications. The device is being considered by auto makers for use in a multiplex system to replace the heavy cable harnesses now commonly used in automobile electrical systems.

RTC-La Radiotechnique Compélec, the principal French subsidiary of Philips, will soon be shipping components produced in what it calls the Mosbip (MOS input and bipolar output) technology. The company's first such product, a 450-V, 10-A switch for use in converters and motor controls, will go into full production next year [*Electronics,* April 19, p. 92].

In Japan, a group at Toshiba Corp., in Kawasaki, is developing a chip comprising C-MOS logic and bipolar transistors to drive electromechanical devices. The present breakdown-voltage capability of 150 V will be extended to 300 V by the end of the year, but only at the expense of current-handling capacity per output transistor. Another Toshiba group is considering Darlington transistors as output devices for smart power ICs, with MOS input stages being used for direct interface with C-MOS logic levels.

NEC Corp.'s Microelectronics Research Laboratory is pursuing two approaches to smart power devices. A high-voltage MOS IC, which consists of 16 n-channel MOS transistors with 400-V, 0.5-A output characteristics and with C-MOS control logic, was developed using a shielded-source structure for its n-MOS transistors. Such a structure suppresses parasitic bipolar effects like latchup. In this smart power chip, the high-impurity-density p^+ ground layer entirely covers the n^+ source layer for its n-MOS transistors.

To realize ICs combining low- and high-voltage devices on the same chip, the two sections must be electrically isolated. The other approach being pursued by NEC engineers is silicon on an insulating substrate.

Sharp Corp., Osaka, manufactures two types of high-voltage display drivers that include diffusion-self-aligned-MOS enhancement-depletion logic circuits. LZ1132, a p-channel part for driving vacuum-fluorescent displays, has a breakdown voltage of 1,000 V, while LZ1032, an n-channel part for driving electroluminescent panels, has a breakdown voltage of 400 V. □

Additional reporting came from C. Cohen, J. Gosch, W. R. Iversen, J. R. Lineback, and L. Waller.

C-MOS and bipolar technologies are more partners than rivals

Rather than competing, C-MOS and bipolar technologies have cooperative roles to play in the advanced VLSI structures of future digital systems

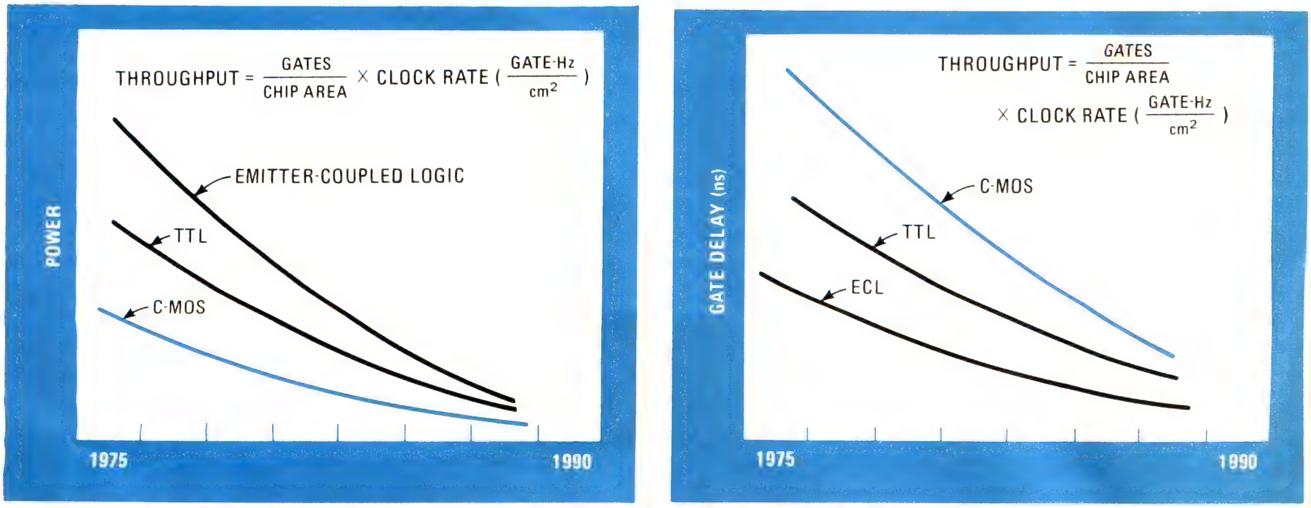
by Bob Stehlin, *Texas Instruments Inc., Dallas, Texas*

☐ In the minds of some observers, the emergence of high-speed complementary-MOS technology for logic-chip applications is sharply dividing the digital integrated-circuit world into two camps. At one outpost, C-MOS will take over low-power medium-speed applications, while the other will be manned by higher-power higher-speed bipolar ICs represented by TTL technology. This view is gaining credibility with the appearance of the HC and HCT families of C-MOS logic, billed as low-power replacements for low-power Schottky TTL (LS) chips. While the simplicity of this scenario is compelling, the battleground is likely to prove more complex.

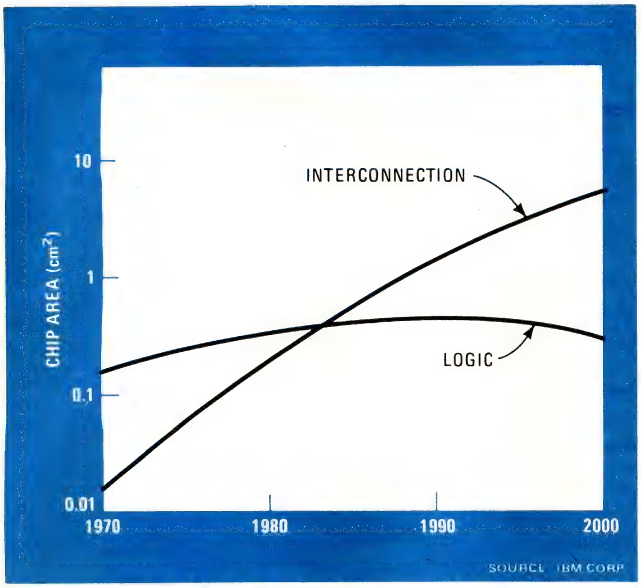
Behind the oversimplifications of the C-MOS versus bipolar issue lie a number of important technology trends whose impact will affect digital ICs far into the future. The first is that higher operating speeds are steering digital technology away from small-scale ICs—glue chips—and towards very large-scale ICs as represented by gate arrays and semicustom and custom chips. While C-MOS technology has improved dramatically and will undoubtedly fill many VLSI applications, bipolar technology has taken strides of its own. Texas Instruments, for example, has put processing technology to work to upgrade the LS and Schottky families, both mainstays of high-performance systems. The result is two new families, advanced low-power Schottky (ALS) and advanced Schottky (AS). ALS chips typically are twice as fast as LS types and dissipate 50% less power. AS devices typically are more than twice as fast as their Schottky counterparts and consume about 40% less power.

As the bipolar speed/power ratio drops and as C-MOS speed improves, processing advances are narrowing the differences between the technologies (Fig. 1). In the future, head-to-head comparisons between them will become outmoded, and a new parameter of evaluation—system throughput—will be more suitable. System throughput includes factors other than speed, like device density (the number of gates per chip area), and line- and capacitance-driving capabilities. Thus it puts technology tradeoffs in a much broader perspective than today's simple speed/power evaluations do.

The ongoing direction of VLSI technology is another reason for giving system considerations more weight. As additional active devices (gates) are packed on chip, the limiting factor becomes not the number of gates that can be squeezed in but the amount of chip area needed to interconnect them. As shown in Fig. 2, interconnection area is now the dominating factor. Since interconnections are essentially transmission lines with resistance, capacitance, and inductance, there is some question about whether C-MOS or bipolar is best suited for line driving. Because bipolar offers higher drive capabilities than does



1. Merge. By the end of the decade, the power consumption (left) and speed capabilities (right) of C-MOS and bipolar technologies will tend to merge. The equation represents a measure of system throughput, a more meaningful parameter for evaluating system performance.



SOURCE: IBM CORP.

2. Filling up. Future VLSI structures will require more area for interconnections than for active devices. While bipolar technology appears to be the best choice for driving long lines, other factors make C-MOS preferable for implementing logic.

C-MOS, it looks like a better choice in VLSI structures. However, other factors enter the picture.

An exploration of the technological differences between C-MOS and bipolar is best begun with an overall view of future directions in digital ICs, provided by classifying all chips as either recursive or nonrecursive structures. In the future, virtually all VLSI circuits will fit one or the other topology. The recursive structure (Fig. 3a) consists of a small number of cells interconnected in a highly ordered manner. Individual cells have minimal internal line capacitance and fan-in/fan-out requirements. Recursive structures are exemplified by memory chips (read-only and random-access memories and so on), structured multipliers, and other functions.

A nonrecursive structure (Fig. 3b) is characterized by a large set of cells having different functions and interconnected with less regularity than a recursive structure. The cells can be interconnected with only a single line, and many cells have large fan-in/fan-out requirements. Most random logic fits the nonrecursive category.

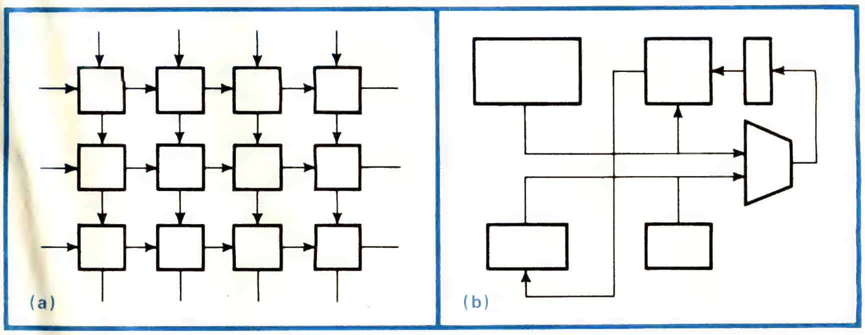
Many of today's SSI and medium-scale system designs will be integrated into single-chip functions—new standard functions, gate arrays, and semicustom and custom chips—most of which are best described as nonrecursive. These structures are bus-oriented, and a large portion of the die area—more than 50%—is dedicated to internal bus lines. Thus a nonrecursive structure follows the trend indicated in Fig. 2—that is, an IC dominated by interconnections rather than active-device area.

Because of their relative speed/power parameters, it comes as no surprise that C-MOS and MOS technologies are more suitable for recursive devices, while bipolar is the better choice in nonrecursive applications. For example, internal cells in recursive structures are well-defined, consistent, and usually have short lead lengths. The characteristics of C-MOS are ideal for such applications, since line-driving needs are less stringent than they are in a nonrecursive environment. Bipolar technology, on the other hand, provides the speed and drive capabilities for driving transmission lines and high fan-in loads—both internal and external to the chip.

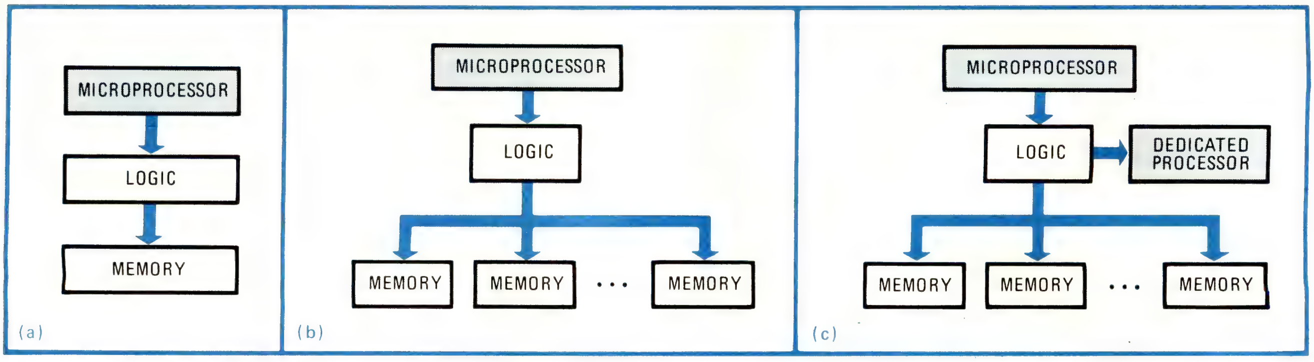
A greater understanding of the roles of bipolar and C-MOS in VLSI structures can begin with the assumption that any digital circuit—recursive or nonrecursive—contains three general types of gate elements. The first type is intended for input/output functions associated with interfacing to other chips in a system. The second is an internal gate that operates in a tightly controlled environment; that is, its fan-in/fan-out demands are minimal. In the third class is the bus driver used for driving elements internal to the VLSI circuit. From the previous discussion, it is clear that I/O and bus-driver gates have characteristics suited to the speed and drive capabilities of bipolar technology. On the other hand, C-MOS is the better choice for internal gate elements.

As is becoming clear, an optimum VLSI chip of the future will take advantage of the best features of C-MOS and bipolar. Inevitably, this points towards mixing both technologies on a single chip to obtain superior performance. Such approaches are already appearing in conference papers and in products available on the market.

Identifying two basic classes of chips that come under this topology can further clarify the nature of nonrecursive structures. These classes are data-manipulation and data-transmission ICs. A data-manipulation IC usually contains from 4 to 18 levels of logic and can contain decision circuitry. At first glance, if the circuit operates at a low clock rate, C-MOS technology may look to be suitable, while a fast clock rate would call for a bipolar implementation. This is not the case, however, since slow clocks are not necessarily associated with a tolerance for long propagation delays between the IC's input and output. For example, if decision logic is integral to the circuit function, the chip will probably require high-speed gates in order to feed information through the decision block. Such gates must have short propagation-delay times because sublevel clock rates can reach frequencies that are



3. Basic structures. VLSI structures can be classified as recursive (a) and nonrecursive (b). A recursive structure is highly regular, with predictable inputs and outputs. A nonrecursive structure is irregular, with varied loading conditions. C-MOS is the choice for recursive elements, while bipolar's drive and speed are needed for nonrecursive elements.



4. Microprocessor-based systems. Three general system categories can be classified by memory and logic requirements. Whether the system is small (a) or large (b and c), most microprocessor and memory functions will be handled by C-MOS technology. But the logic and dedicated-processor functions will most likely be bipolar or a mixture of C-MOS and bipolar.

much higher than those of the system clock.

In general, data-manipulation ICs that must conserve power are candidates for C-MOS technology, while high-performance applications require bipolar. But clock frequency is not an adequate guide for selecting the correct technology. Applications having clock frequencies up to 1 megahertz may seem like clear candidates for C-MOS, but fast decision logic within the circuit will make bipolar a better choice.

When it comes to data-transmission ICs, few tradeoffs are possible, because such circuits are continually sending data out on a bus at high clock rates. High-speed data-transmission chips must have sufficient drive capability to interface with a bus. As opposed to data-manipulation circuits, there is little debate about which technology best fits the data-transmission world. The choice is clearly bipolar.

Real-world systems

Up to now, all of the circuit functions described to implement VLSI chips have been general in nature—recursive and nonrecursive structures, data-manipulation and data-transmission blocks. The three sections of Fig. 4 represent the more specific world of microprocessor-based systems and methods for implementing them.

A small microprocessor system (Fig. 4a) has minimal storage and interface-logic requirements. Since logic is not a dominant factor, such a system lends itself to an all-C-MOS implementation. In the application, the low power consumption of C-MOS coupled with its high noise immunity and wide operating-temperature range make it the optimum solution. It is likely that most small systems of the future in which performance is not paramount will be designed around a C-MOS processor, logic, and static memory.

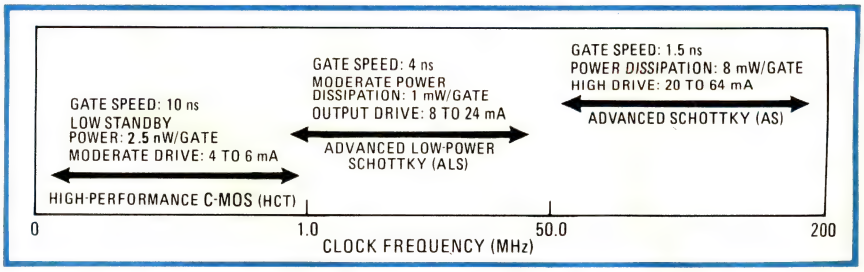
The second type is a microprocessor interfacing to large memory banks (Fig. 4b), such as personal computers, engineering work stations, and front-end processors. Here again, C-MOS technology will dominate in the microprocessor and memory functions. However, the logic requirements for interfacing the processor to memory are much more extensive than with small microprocessor systems. That is, the logic must provide high-performance characteristics (speed and current gain) to drive the memory bus effectively. Bipolar technology best meets the performance requirements of the interface.

The configuration of Fig. 4c illustrates what might be termed the computer system of the future. Such a system supplements the microprocessor with a higher class of computing device called a dedicated, or application, processor. Application processors perform functions such as digital and analog signal processing, I/O handling, and complex arithmetic operations. A distributed processing system of this type has large memory requirements and places a premium on performance, since most application-processor functions are high-speed operations—16 and 32-bit multiplications, calculating fast Fourier transforms, and so on.

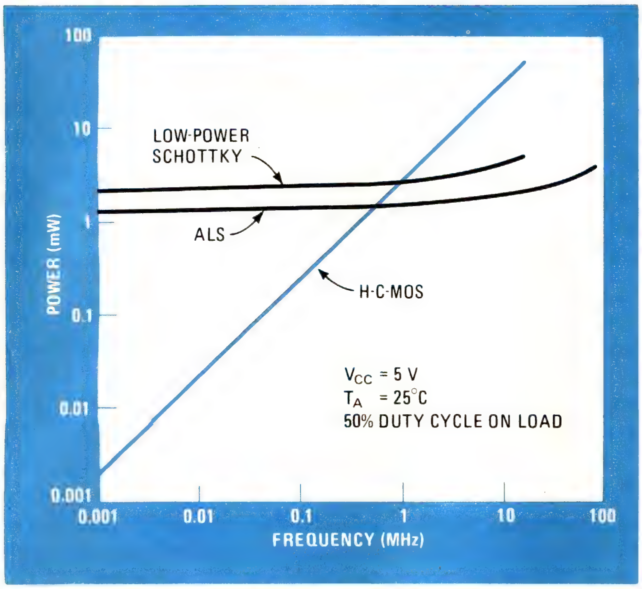
The microprocessor, on the other hand, serves as a system controller, and depending on the overall speed requirements of the system can be C-MOS, bipolar, or a mixture of both. But the interface logic remains in the camp of bipolar because fast switching and line driving are vital in a system that contains both a large memory and a dedicated bus for the application processor.

Although the various systems just described seem commonplace, in reality they depart radically from the configurations of 5 and 10 years ago. In the past decade, system designs were marked by boards using significant numbers of bipolar and C-MOS SSI and MSI devices assembled in random-logic fashion to provide the necessary system functions. Generally, a large number of boards were required to produce a system because of the large number of chips needed.

Matters have changed considerably in the 1980s. The



5. Logic spectrum. Bipolar and C-MOS technology have well-defined operating-frequency ranges. Below 1 MHz, C-MOS reigns supreme, while the high-performance range is bipolar territory. Bipolar devices also show greater drive capability in logic applications



6. Crossover. The curve of the frequency-dependent dissipation properties of C-MOS crosses over the bipolar dissipation curve at about 1 MHz. This allows designers to make speed/power tradeoffs in VLSI structures. In many cases, a mix of both technologies can lead to optimum performance.

new system look has bipolar chips performing the interface logic and I/O functions, C-MOS serving the microprocessor function, and both bipolar and C-MOS application processors to provide the special functions. The memory for such systems is quite large, but isolated on its own boards. To make systems unique, designers can customize the design by using field-programmable logic functions. A programmable ROM contains the firmware to provide the board's operating sequence.

Pros and cons at the chip level

With IC technology headed in the directions described, the basic characteristics and tradeoffs associated with the process technologies become crucial. As noted earlier, the emergence of much higher-speed C-MOS has opened a wide-ranging debate on the implications of this technology for bipolar's future.

First, as Fig. 5 shows, there is a fairly sharp demarcation point, as measured by clock frequency, between the two technologies. HC and HCT C-MOS chips are indeed speed-compatible with conventional LS. But with improved processing and photolithography techniques, ALS offers propagation delay times half those of LS, and lower power dissipation as well. ALS has moved into a higher operating-frequency range than LS, HC, and HCT. In fact, most comparisons of HC and HCT devices versus TTL are based on the specifications of LS, not ALS.

No comparisons between HC and HCT C-MOS against Schottky (S) and its successor, AS, are really possible. Not only was the S version much faster than C-MOS, the AS version is far faster—by more than two times—than the S technology.

Aside from propagation delay, speed-drive capabilities are another factor in a logic chip's ac performance. The primary issue is the amount of external capacitance an IC can drive. Although the drive capabilities of the HC and HCT families have improved significantly —4 milliamperes for standard devices, 6 mA for buffers—they still lag ALS and AS chips. Standard ALS and AS parts can supply 8 and 20 mA, respectively, while certain types of buffers go as high as 24 and 64 mA, respectively. This is one reason why bipolar parts reign supreme for logic applications in microprocessor-based systems.

Excellent noise-immunity has long been a hallmark of C-MOS technology, and this is still true of the HC family. (HCT has the same noise-immunity as LS.) High noise-immunity is an inherent characteristic of C-MOS because its logic states are almost at the level of the power-supply rails. TTL has never been known as a high noise-immunity technology, but considerable strides have been made with ALS and AS logic. This improvement brings these parts much closer to the optimum switching levels, but C-MOS retains clear advantages at the high voltages found in industrial, automotive, and military applications.

Another plus for C-MOS is the extremely low standby power dissipation of the technology. Even with the dramatic improvements provided by ALS and AS chips, C-MOS parts still consume far less power than their TTL equivalents. But the power dissipation of C-MOS is a function of the switching frequency. As long as C-MOS ICs switch at relatively low frequencies, dissipation remains low. The dissipation of bipolar parts, on the other hand, is relatively constant except when the clock frequency reaches its maximum. The power versus frequency curves of Fig. 6 compare H-C-MOS parts against ALS and LS chips.

The key point on these curves is the well-known crossover frequency at which C-MOS and TTL ICs consume equal power. This point occurs at about 1 MHz for H-C-MOS parts operating at a 5-volt supply level. At frequencies above 1 MHz, H-C-MOS continues to draw greater amounts of power, while the dissipation of the ALS chip remains fairly constant until about 20 to 30 MHz. Total system power dissipation is an extremely elusive number, as designers well know. It depends on the number of gates switching at any given time, their switching frequencies, input levels, and the capacitance of inputs and internal bus lines. What is known, however, is that a relatively small number of gates in a system are switching at the maximum frequency at any given time. This means that even in high-performance systems, many of the ICs need not be rated for the maximum switching-rate of the system.

For example, most systems reflect a 70/30 mix of low-power and high-speed logic. That is, in many systems, just 30% of all ICs will switch at the system's maximum frequency, while 70% switch at far lower rates. Thus, in a typical ALS-AS system, 30% of the ICs can be AS types, to meet the highest speed requirements, and 70% can be ALS components for the intermediate to low speeds. Such a ratio helps the designer to meet the system's performance requirements while keeping system dissipation down. The dissipation of the AS parts is about 8 milliwatts per gate, compared with 1.2 mW per ALS gate. Thus 30% of the sockets require the higher-dissipating chips to meet the speed requirements, but 70% of the sockets can take advantage of the relatively high performance and low dissipation of the ALS family. ☐

CICC ranges from floppy-disk controllers to analog custom arrays, laser probing

Other topics at Custom Integrated Circuits Conference include a power process mixing bipolar and MOS, and electrostatic discharge protection for MOS ICs

by Jerry Lyman, *Packaging & Production Editor*

☐ Custom and semicustom digital and analog integrated circuits have become an important factor in today's electronics equation, a development that was highlighted at the sixth annual Custom Integrated Circuits Conference in Rochester, N. Y., May 21–23. The conference continues to grow in scope and stature: 20% of this year's papers came from international contributors. Besides full-custom ICs and semicustom design and gate arrays, the conference heavily emphasized custom integrated-design tools, as well as fabrication technology and applications. In addition, testing and reliability came in with increased contributions over last year.

Custom solutions

Many of the most interesting papers at this year's CICC were in areas where custom ICs stand out and no off-the-shelf types will do. Examples included two papers on ICs for disk-drive controllers and one on a MOS integrated pressure sensor.

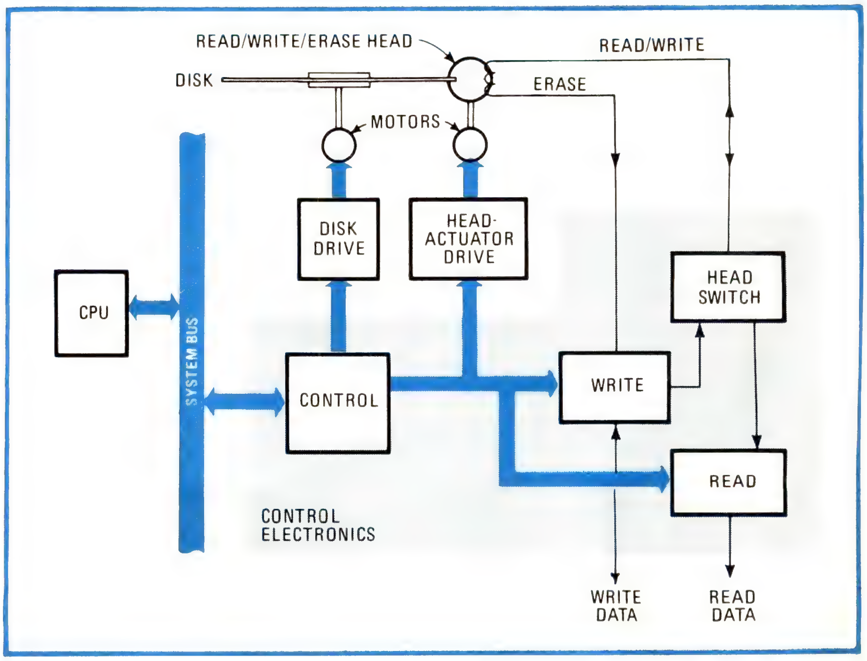
Giving fabrication technology its due, the conference presented a paper on a power process that mixed bipolar and MOS technologies. A paper discussing the critical problem of optimizing electrostatic protection in high-speed MOS very large-scale integration was especially well received.

Analog techniques, overshadowed at most conferences, got their day in the sun at the conference with analog customized arrays coming in for attention in two papers, including one on a high-frequency approach featuring computer-generated custom metalization. In the testing area, one paper described an innovative method of laser probing of IC chips.

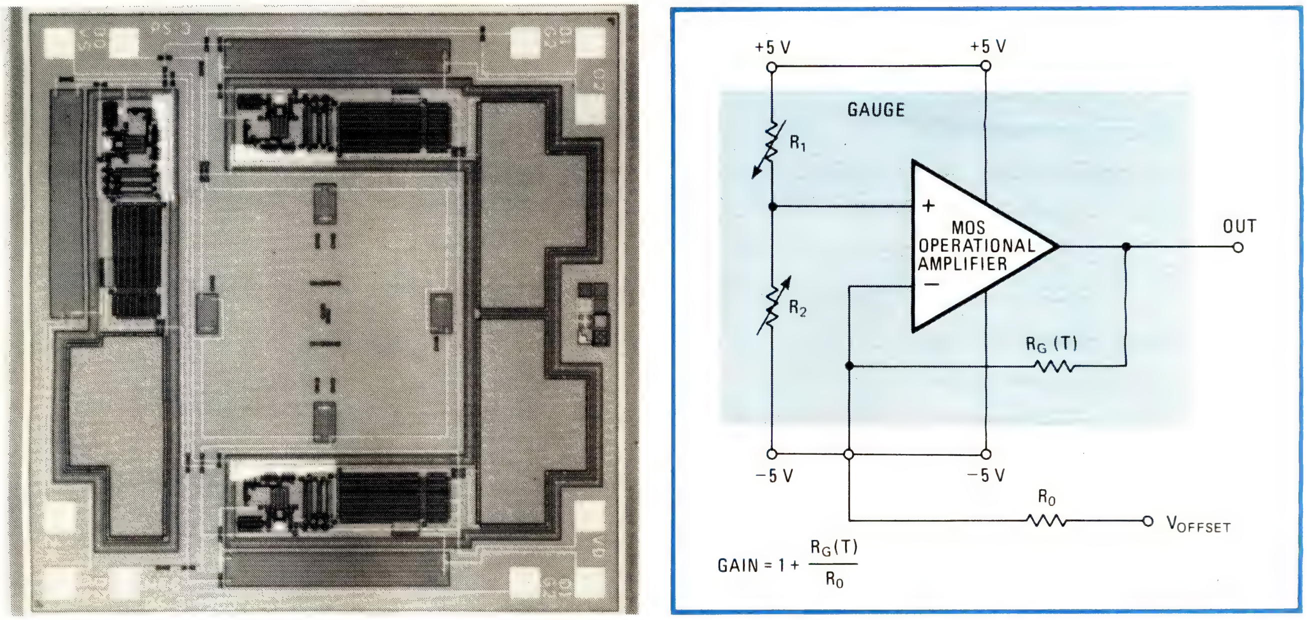
Among the many papers from Japan were two that were especially relevant to today's emphasis on miniaturized disk drives. One, by Tsugutoshi Gotoh and three fellow authors at Mitsubishi Electric Corp., Itami, Hyogo, discussed a single-chip floppy-disk-drive subsystem IC that was designed to squeeze into the limited space that is available in a typical 3½-inch floppy-disk drive. This chip, however, is flexible enough to be applied to a 5¼-in. system.

Figure 1 shows a simplified diagram of a typical floppy-disk drive with the Mitsubishi custom IC's functions within the shaded area. The IC contains the read, write, protection, and erase circuits, plus a pulse generator for the stepping motor, a head switch matrix, timing circuits, and a detector. To compress all these elements, requiring about 1,500 gates, into a 4.54-by-3.76-millimeter chip required a Schottky-TTL process with 3-micrometer structures and multiple-layer metalization. The finished chip comes in a plastic 60-lead quad flat pack.

Another paper, by Nobuyuki Takagi and three co-workers from Toshiba Corp., described a phase-locked-loop IC for magnetic drives. The chip consists of emitter-coupled-logic gates and operates at a data transfer rate of up to 30 megabits a second. The circuitry on the chip consists of two phase comparators and a voltage-controlled oscillator. The IC was designed and fabricated



1. Disk driver. Mitsubishi Electric Corp.'s engineers have put all the circuitry that is needed for a 3½-inch disk drive on one high-density Schottky-TTL chip. All circuitry blocks within the shaded areas are on the firm's new custom chip, which is based on 3-micrometer design rules.



2. Under pressure. NEC Corp.'s MOS integrated diaphragm pressure sensor contains two pressure-sensitive piezoresistors in a half-bridge circuit with a single MOS operational amplifier. The bridge output voltage is amplified with a noninverting feedback circuit.

using an advanced nitride self-aligning process. It includes 110 ECL gates and a total of 1,200 elements on a 2.88-by-2.68-mm chip. The phase drift for the PLL in the temperature range from 0°to 70°C was less than 1 nanosecond. Jitter was also smaller than 1 ns.

This chip could be applied to future magnetic disk drives, which must have high data-transfer rates because of increased recording densities. Furthermore, this PLL could conceivably be applicable to optical disks, video tape recording, and communication circuits.

Still another paper from Japan, on a MOS integrated diaphragm pressure sensor, was authored by Hiroshi Tanigawa and co-workers at NEC Corp., Kawasaki. Previous pressure sensors have used a bipolar construction and were part of a thick-film hybrid.

This custom chip contains two piezoresistors in a half-bridge circuit and a new simple signal-conditioning circuit with a single n-channel MOS operational amplifier. The positive coefficient of the variable-gain amplifier's temperature-sensitive integrated-feedback resistor compensates for the pressure sensor's negative temperature coefficient at the half-bridge.

The pressure sensor was fabricated using standard MOS processes, except for the thin diaphragm formation, which used liquified ammonia anisotropic etchant. In order to minimize induced stress, the silicon wafer was electrostatically attached to a glass plate. A microphotograph of the complete integrated sensor fabricated by the NEC researchers is shown in Fig. 2.

In the sensor circuitry, the p-type piezoresistors (R_1 and R_2), embedded at the diaphragm edges, connect to the half-bridge circuit. Their resistances are changed by applied pressure, which increases one and decreases the other. The bridge output is amplified by the noninverting MOS op amp. Pressure-independent resistor R_G, fabricated by the same process as that used for the piezoresistors, is used in the feedback circuit.

Fabrication, or IC processing, is as important as the application end of the custom-IC business. Perhaps this is why the CICC devoted two sessions to this complex topic: a total of 12 papers dealt with subjects ranging from scaled complementary-MOS technology to bipolar logic gates for ultra large-scale integration techniques.

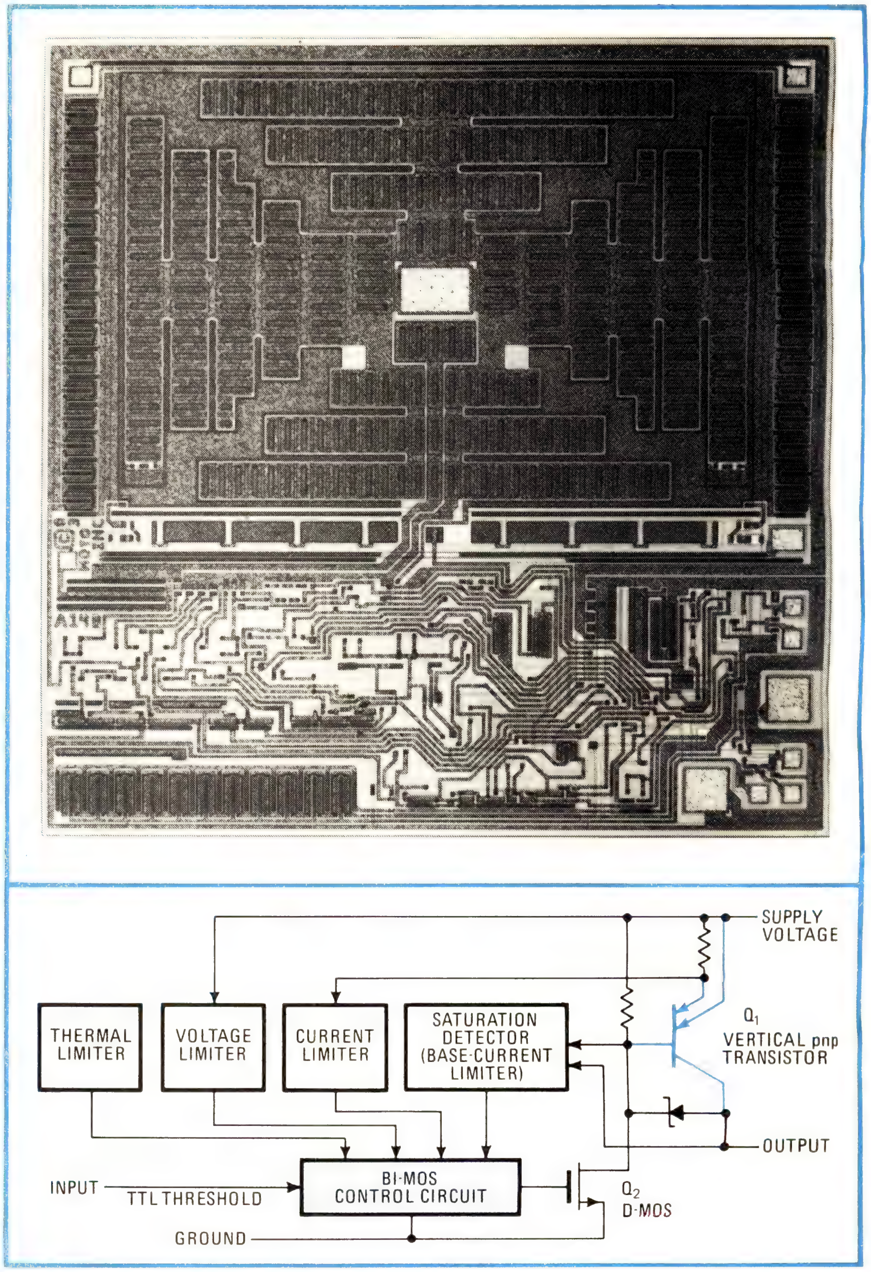
One of the more interesting papers in these two sessions was "Power Bi-MOS—A Versatile IC Technology For Switching and Regulation Applications," by Steven Lytle and colleagues at Motorola Inc.'s Bipolar Technology Center, Mesa, Ariz. The authors noted that switching and regulator circuits should have minimum power dissipation, make efficient use of die area, and be capable of interfacing with digital signals and the loads that they control. Also, other circuit blocks common to power applications must be incorporated when switching high currents. Power bi-MOS incorporates these requirements and can block both positive and negative high-voltage transients.

Taking the power route

Power bi-MOS uses a vertical-power pnp device as the output transistor. This configuration realizes significant advantages. Die area is minimized through the presence of a substrate collector, as this eliminates both the top collector contact area and the lateral spacing needed to maintain high breakdown voltages. Collector-series resistance is decreased by using the package header as the output. Gain characteristics are generally superior to those of a lateral transistor having the same area.

A disadvantage of this design is that during normal operation the epitaxial-substrate junction may be forward-biased. The collector of the power transistor is the output and is therefore at high potential. This causes latching in most standard bipolar designs. To overcome this difficulty, the design utilizes MOS transistors, which are less susceptible to latching in such configurations. In this way, it is possible to design power bi-MOS circuitry that combines the advantages of both high- and low-

3. Bi-MOS. Power bi-MOS combines bipolar and MOS devices with vertical-power pnp devices for minimum power dissipation. A high-side driver that uses this process can drive loads to within a few hundred millivolts of the supply voltage.



voltage MOS and bipolar chips.

In bi-MOS processing, a substrate pnp power transistor, bipolar analog devices, and metal-gate 7-μm C-MOS field-effect transistors are fabricated in 10 masking steps. The first product to be implemented in this technology is a high-side driver. The circuit (Fig. 3) has TTL-compatible inputs and can drive loads to within a few hundred millivolts of the supply voltage. It incorporates all the features usually found in power ICs, among them voltage and thermal shutdown, current limiting, and a saturation detector. Lateral pnp transistors and laterally diffused MOS transistors block negative and positive 125-V transients, respectively.

A paper that should have been a must for anyone using high-speed MOS VLSI was "Optimized ESD Protection Circuits For High-Speed MOS VLSI," by Eric Fujishin and co-workers at Zilog Inc., Campbell, Calif., and Mark D. Hartranft, Cypress Semiconductor Corp., in Santa Clara, Calif. This paper described new electrostatic-discharge-protection circuits for MOS VLSI chips, which provide a typical 2.7-ns delay and protection against 2,200-volt transient spikes. In addition, for use with C-MOS circuitry these circuits are immune to latchup.

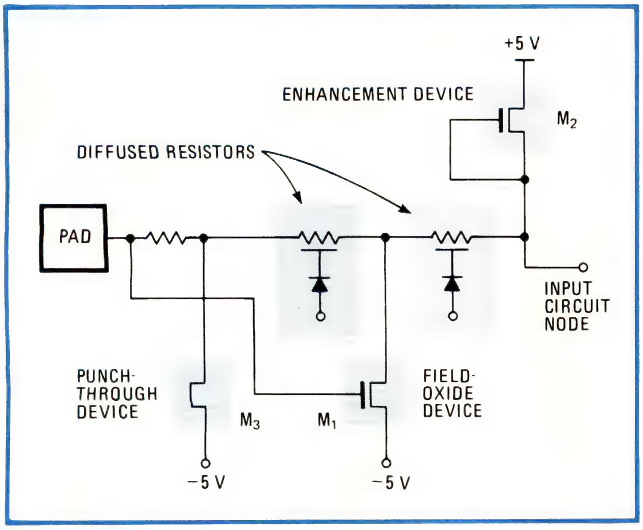
Previous electrostatic-discharge-protection circuits guarded against pulses from 20 V to more than 1,000 V. With the increasingly thinner gate oxides used in VLSI, however, these circuits fail to protect adequately against low-voltage pulses. Also, the delay times associated with such circuits add significantly to the access times of their parent chips, calling for a completely new approach.

Figure 4 shows the new basic electrostatic-discharge-protection structure designed for input protection of VLSI chips. The basic circuit contains not only traditional diffused resistors (distributed diodes), a thick-oxide punch-through structure (M_3), and a FET (M_1) but also a thin-oxide device (M_2) operating in saturation for low-voltage protection.

For positive pulses, the thick-oxide FET (M_1) protects against rapid high-voltage electrostatic-discharge pulses. With the gate tied to the input pad, this device is driven by the electrostatic-discharge pulse and turns on instantaneously to provide a low-resistance path to V_{SS}. The threshold voltage of the field-oxide device, however, is between 20 and 30 V and provides no protection against low-voltage transients. The punch-through device also fails to offer low-voltage protection. In contrast, however, the thin-oxide device (M_2), which turns on at 1 V or less, does provide the needed protection against low-voltage pulses.

Negative pulse protection is provided by the diffused resistor, which acts as a forward-biased diode to the substrate. Additional protection is added by parasitic npn bipolar transistors with reverse-biased collector-base junctions (source-substrate of M_1 and M_3) and forward-biased emitter-base junctions (drain-substrate of M_1 and M_3), placing these devices in a forward active mode and providing other low-resistance paths to V_{SS}.

Test vehicles containing the new input-protection circuitry were fabricated using a 2-μm n-MOS process with gate thicknesses of 350 angstroms. Results indicated



4. The protector. This MOS electrostatic-discharge-protection network built with a thick-oxide field transistor, a punch-through device, a thin-oxide enhancement device, plus diffused resistors (distributed diodes) can survive up to 2,200-V spikes with a response of 2.7 ns.

that protection levels above 1,200 V could be achieved under all conditions.

An innovative paper in the session on analog techniques by Winthrop Gross of Tektronix Inc., Beaverton, Ore., described the Quick-chip, a kind of analog gate array. The paper described a system for fast design and inexpensive prototyping of high-speed analog chips with a good chance of first-time success. Furthermore, the Textronix system is constructed for use by circuit designers who are basically unfamiliar with the intricacies of integrated circuitry.

The Quick-chip system consists of a very high-frequency IC fabrication process; a core comprising a mix of transistors, resistors, and layout features suitable for remetalization; a user's guide; a library of Spice computer-simulated models for the core IC; a grid-based layout system; and a graphics-layout editor. The system has been used to prototype over 30 circuits, most of them by circuit designers with no IC experience. The original Quick-chip has 18 npn transistors per chip and 13 tapped, implanted resistors in addition to one Nichrome thin-film resistor.

A bigger Quick-chip

Quick-chip has proven so successful that Tektronix is designing a larger core circuit with about 200 npn devices for remetalization. The new design will also incorporate lateral pnp devices for low-capacitance pullups, implanted resistors with high sheet resistance, and user-programmable MOS and junction capacitors.

Perhaps the most exciting paper of the entire conference was "Testing and Failure Analysis of VLSI Using a Laser Probe," by Francois J. Henley of Spectrum Sciences, Santa Clara. Noncontact methods such as electron-beam and laser probing have been proposed as a substitute for cumbersome mechanical probing in design debugging, failure analysis, and characterization work. But until recently, laser probing suffered from serious speed and signal-detection problems, which offset its inherent simplicity (no need for vacuums, feed-throughs, or removal of a passivation layer) and nondestructive nature. Spectrum Sciences therefore designed its laser prober to incorporate a measurement scheme that allows high-speed-logic state analysis (at tens-of-megahertz test speeds), useful for detecting critical path- and race-condition problems.

The prober measures a particular node's state information by illuminating the transistor with a focused laser spot and monitoring the power-supply pin. It can be shown that the magnitude of the measured photocurrents is a function of the state of the transistor being illuminated. By scanning the measured photocurrent for succeeding states, computer processing can extract the corresponding logic diagram.

Spectrum Sciences put its prototype of the laser prober through its paces in order to demonstrate the unit's ability to do high-speed testing. The prober has an acousto-optically switched helium-neon continuous-wave laser focused to a 2-μm spot as the state analysis source. The paper presented at the CICC gave example analyses on C-MOS microprocessors.

The presentation of some two dozen papers on computer-aided design underscored the conference's stress on this subject. Among the standouts, one paper focused on the automatic layout of gate arrays and another on the extraction of interconnection delays from computer-generated layouts.

In the paper on gate-array layout, Jeong-Tyng Li and others at the Electronics Research Laboratory, University of California, Berkeley, described an automatic layout system for gate arrays that incorporates novel and efficient algorithms for placement and routing. The system, called Bagel, has four main components: a data-base library, placement, a global router, and a detailed router. The system has processed a 2,000-gate array in 35 minutes of central-processing-unit time.

Checking interconnections

In the second CAD paper, Joseph D. Mastroianni of the RCA Solid State Technology Center, Somerville, N. J., pointed out that state-of-the-art algorithms for the automatic placement and routing of cell-based designs do not take electrical parameters into account during layout realization. As a result, a layout that might be best from a purely topological standpoint still might not function optimally because of parasitics introduced by interconnection. The author went on to note that this problem is especially critical in the high-volume, fast-turnaround world of semicustom chips.

Mastronianni's paper detailed the algorithms and interfaces of a point-to-point delay-calculation system that is used to calculate the effects of interconnection loading on automatically generated cell-based designs. The program characterizes interconnections as an RC tree and calculates point-to-point delays for each of the nodes on a chip. The output feeds directly to RCA's Mimic logic simulator and is filtered by a user-defined set of thresholds that prevent the proliferation of nodal data. This program is part of RCA's Quick Turnaround semicustom design system and is integrated into the layout-verification system. ☐

As packaging density increases, focus shifts to SSI and MSI chips

Experimental three-to-four-chip packages hold much promise, but IC houses must work to make standard assemblies available

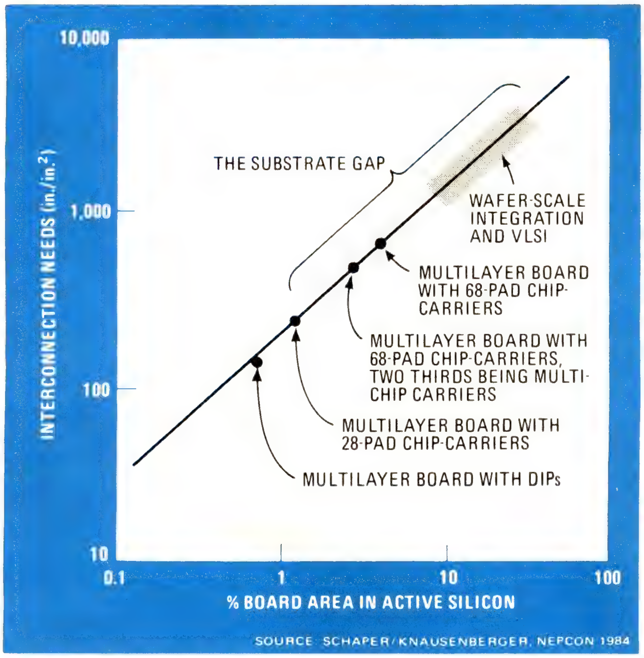
by John W. Balde, *Interconnection Decision Consulting, Flemington, N. J.*

☐ Tremendous strides in system-packaging density have been made in the past few years, driven by the functional and density advances of large-scale and very large-scale integrated circuits. The use of LSI and VLSI chips has reduced system size by about 10 : 1, both in memory boards and in logic, even with many of the small- and medium-scale integrated circuits still in dual in-line packages. Additional reductions in size and cost of boards and systems have been made possible by the shift from DIPs to chip-carriers and pin-grid arrays.

Now attention is shifting to the remaining SSI and MSI circuits still packaged in DIPs. How these interface chips are to be packaged is the important issue, since it is improvements here that will make possible the coming reductions in board and system sizes.

Today, application of VLSI in most computers is restricted to about 80% of the total circuitry because of high chip-design costs. The remaining SSI and MSI chip packages so influence the board design that many computer-system designers have hesitated to shift into full surface-attached technology or some other form of cost-effective packaging. Until SSI and MSI circuits are also packaged efficiently, many of the board-packing advantages of the new technology are still absent.

Theoretical studies of the possible benefits of increasing packaging density usually assume a complete shift to some new technology, either chip-carriers or pin-grid arrays. Since this is rarely the case, typical densities are therefore much lower than these studies indicate. In the diagram of packaging densities (Fig. 1), recently presented at Nepcon West by L. W. Schaper and W. H. Knausenberger of AT&T Bell Laboratories, Whippany, N. J., the superior performance of surface attachment is based on the assumption that all chips are packaged in identical chip-carriers. They cited an example using packages with 28 input/output pads: if the same circuitry could be mounted on a board using packages with 68 I/O pads, the density improves significantly, as the figure shows. However, this is not likely if all packages are to be filled with LSI and VLSI chips, whose design must be justified economically.



SOURCE: SCHAPER/KNAUSENBERGER, NEPCON 1984

1. Substrate efficiency. Multichip carriers can raise interconnection density. For example, using chip-carriers with 68 I/O pads, two thirds holding four SSI and MSI chips each and a third with LSI chips, hikes density over a board of carriers with 28 I/O-pads.

Multichip assemblies

An efficient solution for the smaller circuits has been proposed for some time: package the smaller chips in groups. In the case of memory chips, the single in-line package has been used to create a multichip memory unit. This is a practical package for memory, because of the relatively small number of I/O leads and the ability of memory circuits to tolerate some additional lead length and circuit delay. However, to meet the needs of logic and general-purpose chips, something else is needed.

The solution is to package a portion of the glue circuits—the lower-technology silicon needed to hook things together—into the same package type and size used for the LSI and VLSI chips. This was advocated as early as 1980 [*Electronics*, Jan. 17, 1980, p. 113), but is only now becoming accepted as an appropriate solution. Quite recently, Hughes and AT&T have joined RCA, IBM, and Sperry in using this approach.

What this technology could do to package density is considerable. Using 68-lead packages, a third with LSI chips and two thirds being multichip, density is improved significantly.

The question then is

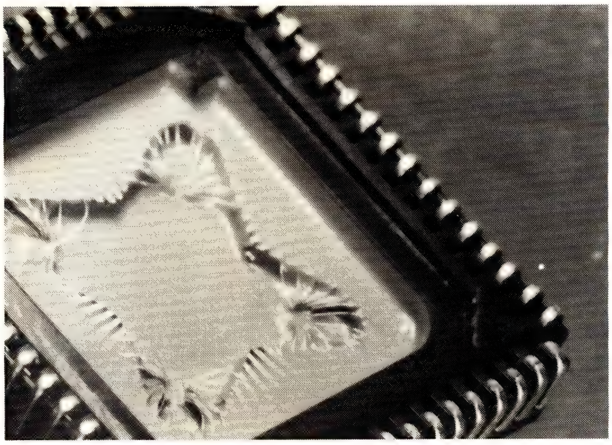
why there has been no big shift to multichip packages. The answer is that IC manufacturers do not want to sell uncased chips, which are difficult to test and to handle safely. And there is always the issue of responsibility for defects that are found by the customer after the chip is mounted.

There is another factor—one that some IC houses deny, but which must be a consideration in the price-and-profit structure of the IC marketplace. High-performance LSI and VLSI chips are fairly expensive and are always priced at levels considerably higher than those of their packaging—even in the case of some pin-grid arrays where the packages cost $16 to $20. SSI and MSI chips, however, are very price-competitive, and the packaging operation may produce a profit comparable to the profit on the chip itself. Sell the chip without the package, and a significant source of profit for the IC manufacturer disappears.

IC manufacturers do not want to sell postmolded multichip packages either, even though these firms have large capital investments in molding equipment. The reason is that postmolding is not really suitable for these chips. Postmolded multichip packages would be costly, because the yield problem would be severe. Since some of the chips will fail during burn-in and testing, there has to be a way of changing bad chips to repair defective assemblies, which is not possible in postmolded packages. For all these reasons, multichip packages are not a major product of the IC houses.

Some original-equipment manufacturers have resorted to multiple-IC packaging with purchased uncased chips, but often they have used larger hybrids with more chips. This does not appear to be a good general solution: the bigger the hybrid, the less likely it is to be manufactured with standard inner wiring and standard chips. Another advantage of small three- or four-chip packages is the likelihood of such a small cluster of chips being replaced by some standard mass-produced chip before the system reaches volume production, further lowering the IC cost.

To be readily available as a stock item, therefore, the three-to-four-chip package should not be "special." The package must bring all the leads out separately to the I/O pads or pins, not only so the chips can be tested, but to make the package independent of chip contents.



2. Premolded. The open premolded chip-carrier is suitable for housing three to four chips. In this AMP experimental package, defective chips that might turn up in test or burn-in could be replaced easily. In the postmolded chip-carrier, no repair is possible.

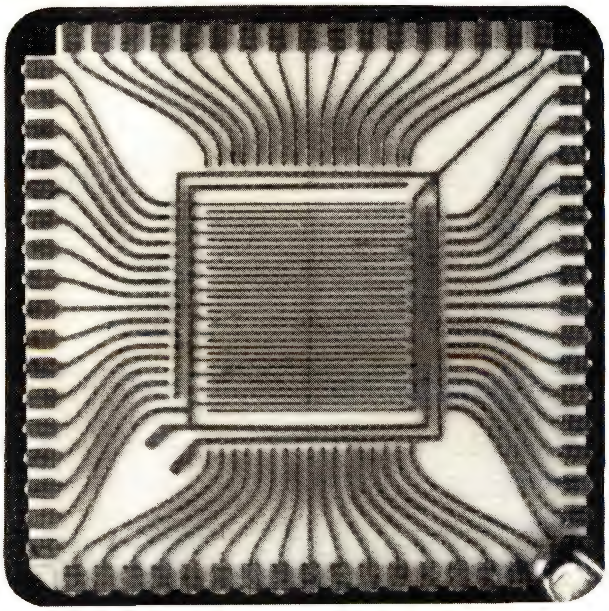
One solution is to shift to an open package, either leaded ceramic or an open premolded package. Then up to four SSI and MSI chips can be installed in the same package size used for LSI and VLSI chips (Fig. 2). Furthermore, the leads can be brought out separately so that a standard package can be used. This methodology does require a purchased package, but the advantage to the OEM can support the slight cost involved.

The important thing is that, whatever the package, its size must be the same as that of the largest VLSI chips on the board. With a uniform array of packages, the task of computer-aided board layout becomes very similar to that of the design layout of an IC chip itself. There is a great similarity between gate-array or standard-cell VLSI design and a subsequent printed-circuit-board layout of 30 or 40 square packages with an identical I/O footprint. There will be a significant simplification of the interconnection-substrate design if the same algorithms can be used for pc and IC-chip design.

What is needed is for the IC houses themselves to take the initiative by willingly providing small multichip assemblies. Texas Instruments Inc. has said that it will do this, but there seems to be little action by it or others to provide standard packages. System OEMs cannot really do the job, since a design cannot pass their own review acceptance if it requires waiting for an IC house to begin such an operation. The other option, to set up a hybrid facility, also poses an undesirable delay for the average OEM.

So the need persists. If the package and the chips inside were standard types, the board and system would enjoy a 2 : 1 or greater improvement in packaging density, with proportionally reduced costs—a potential boon to the first IC house that pursues this market aggressively.

The question is whether



3. Power rings. For power and high-speed applications, the resistance and inductance of the thick-film conductors of a substrate are too high. This AMP substrate has low-impedance copper conductors and two rings for power and ground wire bonds.

the approach used in the multichip premolded plastic chip-carrier can be implemented equally easily in ceramic leadless chip-carriers or pin-grid arrays. Some existing ceramic chip-carriers can mount multiple chips, and certainly IBM has used pin-grid arrays for their multiple-chip substrates. But this does not mean that all packages work equally well, since it appears that the chip-carrier offers the classic case of "bigger on the inside and smaller on the outside."

Raytheon Co., Lexington, Mass., has shown that the chip-carrier takes up less board space and has more chip area than pin-grid arrays with up to 400 I/O leads. More important, it is easier to bring the leads out to the edge of a peripheral-lead carrier than to route them through the field of pins from the bonding pads at the edge of the chip. This is particularly true when routing leads from four chips. Chip-carriers require fewer layers of package and pc substrates than the pin-grid arrays, which have a reduced signal-wiring capability per layer because of the vias and pads around each pin.

Power and ground needs

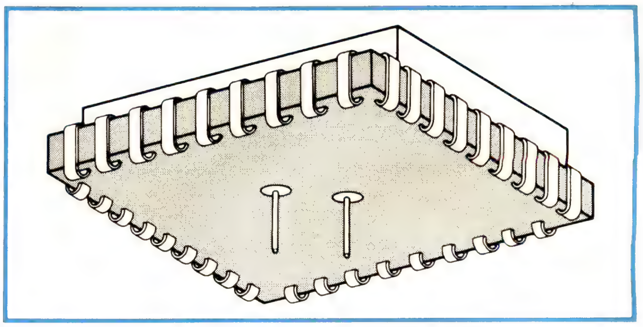
Another consideration in the choice of the multichip package is its ability to handle an increasing number of I/O leads. Some experts argue that the pin-grid array has no upper limit, whereas chip-carriers, even with I/O pads on 20-mil centers, will be limited to about 260 leads. But this may not be a fair comparison. Typically, up to 25% of the package's I/O leads are devoted to multiple power and ground leads, because the series resistance and inductance of any one lead is a serious limitation when high-speed circuits are required. If only one power or ground lead is used, the common impedance will produce common-mode crosstalk. Using multiple leads reduces the common impedance and hence the crosstalk. For example, a 260-lead device may have only 180 signal leads, all others being multiple power and ground.

This paralleling of leads can be avoided by using two surface-bonding square buses inside the package, as in the AMP ceramic chip-carrier of Fig. 3. Connection to external power and ground with only two leads is feasible if those leads are low in resistance and impedance. This would eliminate the use of tungsten or molybdenum for the connection circuits on the chip package. Thin- or thick-film conductors would have excessive resistance. Thus copper is required, either in a pre- or postmolded lead frame, or in the leaded ceramic chip-carrier.

Beryllium-copper, whose resistance is 10 times that of plain copper, and Alloy 42 or other iron-based alloys with 100 times the resistance, can be a problem. With an iron-alloy series resistance of about 200 milliohms in a 6-watt device and a 3-volt supply, there will be a drop of 400 millivolts—a significant percentage of the signal swing. Shifting to copper leads and conductors reduces this drop to an insignificant 4 mV.

With chip-power dissipation going from 4 to 6 W and supply voltage dropping from 5 to 3 V, currents of 2 amperes are likely. Lead resistances of 200 mΩ are excessively high, resulting in significant voltage drops. Only copper leads are sufficiently conductive to permit abandoning multiple lead connections.

Furthermore, the copper must extend all the way to the bonding ring, without any intervening thick- or thin-film conductors. This suggests also that a pin-grid array with a pc-material substrate can do the job better than current ceramic ones, or that the power and ground rails need to be handled separately in a very low-resistance, low-inductance manner.



4. Pinned to the board. A proposed composite ceramic package would use two pins connected internally to two square rings to bring out power and ground leads. Signals would come out to the compliant leads. This method reduces the number of output leads needed.

An alternative to the pin-grid array or chip-carrier could be a new package (Fig. 4) that combines the pin connections for power and ground with the edge leads of the leaded chip-carriers. Here, two pins brazed on the bottom of the package can be inserted in holes in a pc board and provide a low-impedance power-and-ground connection, while the flexible edge leads conforming to a standard chip-carrier outline can provide signal connections. (Two holes every 2 square inches are a trivial routing penalty, much less than the 200 to 400 holes required in a board for a pin-grid array.)

Inside the package, the power and ground pins connect to the two concentric rings, where multiple wire bonds are made from the chips' I/O pads. Any decoupling capacitors required can be attached right at the connection points of the pins to the rings.

Pins plus leads

In a typical application, the user would insert the two pins in holes in the substrate, without soldering. Then the peripheral leads would be soldered in the same manner as a leaded chip-carrier, followed by manual soldering of the two pins. Another option would be to reflow-solder the peripheral leads and simultaneously melt preforms to solder the power pins. Socketing is also possible, with the pins providing alignment keys.

At this point, it may not even be necessary to introduce a new package. If plastic packages are anticipated (as they would be for 80% of future packaging), then their inherently low-resistance copper leads are fine, especially if the inductance of the power and ground leads is minimized by tightly coupling the leads to provide high mutual inductance and low self-inductance. The same applies to copper-leaded ceramic packages—just shift to copper-bonded leads.

These four chip packages, in ceramic or plastic premolded cases, offer much promise for the reduction of system size and cost. But only when standard packages are available will most system manufacturers be able to take advantage of them. ☐

Engineer's newsletter

Report to survey Japanese packaging

Opening up one of the latest Japanese calculators, cameras, or video cassette recorders makes it quite evident that Japanese engineers are among the leaders in innovative electronic packaging. But a comprehensive report on what the Japanese are doing in this vital area has never been available. To fill this need, D. Brown Associates Inc. is preparing a major study of electronic packaging in Japan. **The report will cover the efforts of more than 20 major electronic-equipment manufacturers in the computer, telecommunications, and consumer fields,** plus look at more than 10 component suppliers. It will be available in February 1985. The prepublication price is about $10,000; after publication, the report will sell for about $11,000. For details, write to D. Brown Associates Inc., P. O. Box 43, Warrington, Pa. 18976 or call (215) 343-0123.

NBS set to study sodium poisoning of semiconductors

Researchers at the National Bureau of Standards Center for Analytical Chemistry, Washington, D. C., are using the bureau's 10-MW reactor to study how sodium ions cause semiconductors to fail. Sodium can migrate in semiconductors, causing bridges that poison the chips and render them ineffective. To examine this process, **NBS scientists are doping samples with sodium to simulate conditions found during the manufacture and operation of semiconductors.** Then, using a nondestructive technique called neutron depth profiling (NDP), they are exposing doped samples to a beam of neutrons from the reactor. With this procedure, a map can be made that profiles the depth distribution of sodium in the samples. Data from the NDP research will be used by manufacturers to design barriers for blocking sodium.

HP develops an alternative to the clean room

The days of the clean room may be numbered. Hewlett-Packard Co. has developed a technology that may make it possible to produce chips in a normal room environment with workers wearing regular clothing. **The HP technique, called a standard mechanical interface (SMIF), uses small dust-proof boxes to transport wafers**. A specially designed trapdoor is used to transfer the wafers to and from chip-processing machines without contamination. HP's initial tests indicate that the cleanliness of chip making could be improved a hundredfold with the new technology. For example, the typical clean room operates with an average of 100 particles in each cubic foot of air. Early tests of the new HP technique indicate that the inside of the transport boxes can be kept at a level equivalent to one particle per cubic foot of air. SMIF was conceived at the HP Laboratories in Palo Alto, Calif., and is currently being installed at HP's chip-making facility in Corvallis, Ore.

EIA expands standards for surface mounting

An expanded version of EIA RS-481, "Taping of Surface Mounted Components for Automatic Placement," has passed the Electronic Industries Association's Automatic Component Processing and Insertion Committee. **This revision encompasses those dimensions and tolerances needed to tape electronic components of various sizes using 12-, 16-, 24-, 32-, and 44-mm tapes,** in addition to the 8-mm tape defined in the existing standard. The revised standard for 8-to-44-mm tape covers use of 8-to-20-lead small-outline IC packages, 12-to-40-pad leadless ceramic chip-carriers, and 18-to-44-pin leaded chip-carriers, plus chip capacitors, chip resistors, and related passive components. **–Jerry Lyman**

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Thin-film transistors drive pixels singly

Liquid-crystal display uses active matrix addressing to achieve higher performance capabilities and lower power consumption

by Wesley R. Iversen, Chicago bureau manager

The focus of recent work in flat-panel-display technology has been on what is called active matrix addressing, in which such active devices as thin-film transistors are fabricated directly on a display substrate for driving picture elements on a one-to-one basis. This technique overcomes many performance limitations associated with traditional addressing schemes and has been the basis for experimental displays and miniature-TV prototypes developed by a number of Japanese companies [*Electronics,* Oct. 6, 1983, p. 101].

Now a Pittsburgh start-up known as Panelvision Corp. is bringing out a display based on this technique. Called the MiniGraphic, the display relies on 24,576 cadmium selenide thin-film transistors fabricated on a glass substrate for driving a twisted-nematic liquid-crystal display. Together with a board clamped and sealed to the back of the display and containing complementary-MOS driver chips, the MiniGraphic measures about ½ in. thick.

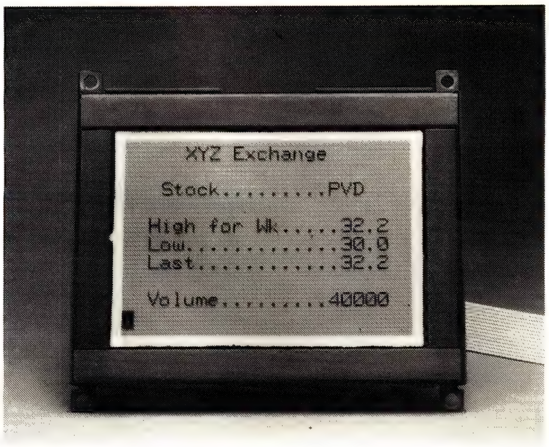
With one cadmium selenide transistor for each of the pixels (arranged in 128 rows by 192 columns), the MiniGraphic offers a 3.84-by-2.56-in. display area that can handle from 12 to 16 rows of 32 characters each. This is probably not large enough to find widespread use in portable computers, which are likely to require a minimum of 40 characters per line, concedes Thomas C. Maloney, Panelvision marketing vice president.

The firm will later address that market with larger displays, but it foresees a number of applications for its first product, including medical and scientific instruments, remote teller terminals, point-of-sale equipment, process-control panels, and automotive and aircraft instruments.

The initial MiniGraphic will provide a black and white display only. But with the addition of some analog circuitry, a gray-scale option could be provided on subsequent products, the firm says.

Avoiding problems. By providing direct transistor driving at each LCD pixel site, the MiniGraphic aims to avoid problems inherent in conventional multiplexed addressing schemes in which a pixel is illuminated when the combined voltage of signals sent down the appropriate rows and columns of electrodes exceeds a certain value. This method requires precise voltage control, which can increase the cost and complexity of a system, says Panelvision. Also, since the pixels can fade between refresh cycles, it imposes practical limits on display size, contrast ratios, viewing angles, response speeds, and other performance features.

By contrast, active matrix addressing generates a near-100% duty cycle by providing, at each pixel, a storage capacitor that maintains full saturation voltage on the display material between addressing cycles. Whereas conventionally addressed twisted-nematic LCDs typically offer contrast ratios in the 3 : 1 range and a 30° viewing angle in one direction, for example, the MiniGraphic comes with an 8 : 1 contrast ratio and provides a 45° viewing angle in all directions.



By combining active matrix addressing with a passive display material such as liquid crystals, power requirements are also kept low. Operating from a 5-V supply, total power consumption for the MiniGraphic display (including the attached driver-chip board) and an additional required circuit known as the voltage-level shifter (which converts the 5-V supply to the 18-V levels needed to drive the transistor gates) is said to be 50 mW maximum.

An optional controller board will take about an additional 2 W, says Maloney. Like the MiniGraphic display, the controller board requires only a 5-V supply for operation. Equipped with an Intel 8031 microcomputer, an on-board character generator, and a bit-mapped refresh memory, the controller is designed to handle MiniGraphic functions based on software commands from a host processor.

The MiniGraphic will be unveiled at the Society for Information Display's 1984 symposium in Dallas next month, and is set for production availability in August. In 500-unit quantities, the standard reflective version will sell initially at $360 per unit (including a separate voltage-level shifter) without a controller board. With the controller board, the price is $700 each in the same quantities. A backlit, or transflexive, version will sell for a $50 premium.

Panelvision Corp., 265 Kappa Dr., Pittsburgh, Pa. 15238. Phone (412) 963-9635 [Circle reader service number 338]

Reflow-soldering system for surface mounting uses thermal mass to prevent vapor collapse

Because vapor-phase technology is quicker and causes less thermal stress than approaches involving radiant or convection heating, it is expected to find increasing use for reflow soldering. Indeed, says Robert Cox, marketing manager for Corpane Industries Inc., vapor-phase soldering holds particular potential in surface-mounting applications because the vapor can penetrate between densely packed components on a board and thus uniformly apply heat at solder reflow temperatures.

Now Corpane is looking to capitalize on the trend toward surface mounting with a vapor-phase-soldering system that the 10-year-old Louisville, Ky., firm says can reduce operating costs by as much as 80% over conventional vapor-phase techniques. What's more, the firm contends that improved vapor control gives its system higher production rates, as well as better product quality, reliability, and yield.

One key to Corpane's approach is the use of a thermal mass, such as a molten liquid, to supply the heat necessary to boil the liquid (commonly Fluorinert or Flutec) and produce the vapor. In a vapor-reflow system, assemblies moving through it act as condensors for the vapor, which heats the solder on the board holding the assemblies to reflow temperatures and then runs off in liquid form. In conventional systems, this cooled liquid runs into a pool of boiling liquid, which is heated by immersed, electrically controlled heaters.

A problem with conventional vapor-phase soldering systems is that the cooled liquid reduces the vapor-generation rate, requiring additional heat to maintain the liquid boiling rate, explains Corpane project-development engineer Michael J. Ruckriegel. This takes a great deal of energy and can mean that the boiling rate is much higher than would be needed to maintain the standing vapor zone. Furthermore, says Ruckriegel, conventional systems cannot supply the instantaneous additional heat required to maintain the standing vapor demand—particularly during the initial stages of assembly immersion—which means that vapor collapse is quite common.

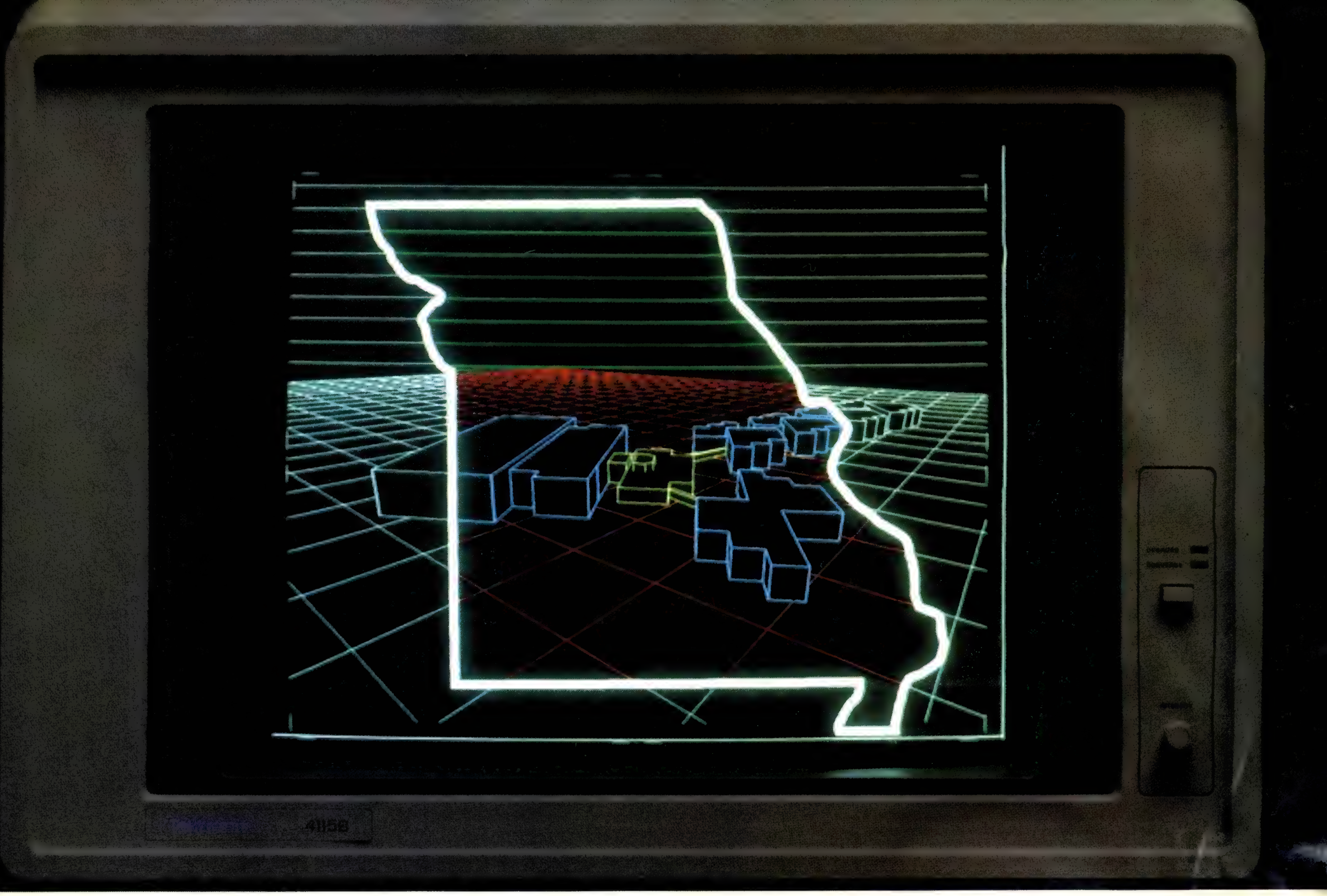
The Corpane system, however, substitutes the molten liquid's thermal mass, so that no standing liquid is maintained. When the condensate runs off, the reserved heat it contains causes it to reboil as soon as it contacts the molten liquid. Like the boiling liquid in conventional soldering systems, the molten liquid in the Corpane system is heated by electrically controlled heaters, but it is reheated during low-demand cycle times.

The result is that vapor collapse is practically eliminated, according to the company, while power requirements are some 70% lower than they are for conventional systems. In addition, the system requires much less starting fluid.

Significant savings. Since no standing liquid is maintained, a Corpane system for a 24-by-24-in. printed-circuit board would require only 1 gallon of fluid, compared with 10 to 16 gal. in a conventional system. This can result in significant cost savings, says Cox, since fluid expenses can typically amount to more than $700/gal.

Besides the thermal-mass method (which the firm is attempting to patent), the Corpane system applies other techniques to save money and boost system reliability and soldered-board yields. These include the use of a patented vapor-control weir for upper-zone vapor control instead of the wrap-around cooling coils common in conventional systems. Since the cooling apparatus is placed behind the weir in the Corpane system and not exposed to air, contamination from condensation is practically eliminated, the firm says, while fluid loss is also reduced. The Corpane system also has programmable controls with full-system sensing to reduce losses further by accelerating or decelerating pc-board movement into and out of the vapor zone and by establishing proper dwell times.

Corpane plans to offer batch models of its system, as well as in-line systems for conveyor-based continuous-feed production. The four batch models are available now and range in price from about $40,000 to about $65,000, for systems that handle boards of up to 12 by 14 in. and



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24 by 24 in., respectively. Typical board cycle times are about 30 s in the batch models, which use a secondary vapor above the primary vapor for system control.

The in-line systems will be available in July in both double- and single-vapor versions. Pricing on the in-line systems ranges from about $60,000 to $100,000 or more depending on a customer's need for special wiring and other options, Cox says. The maximum conveyor speed on each of the six in-line models is 8 ft/min.

Corpane Industries Inc., 250 Production Ct., Louisville, Ky. 40299. Phone (502) 491-4433 [Circle 339]

Modular tool kit brings C language to real-time multitasking applications

With its introduction of the Csharp Realtime Toolkit, the Systems Guild, a year-old start-up, is bringing the C programming language into the real-time, multitasking world. Available in a version for use on the entire PDP-11 processor family, as well as in a generic version for other 8- and 16-bit microprocessors, Csharp is distributed in source code, and users may modify it at will.

"In real-time environments, it is important for programmers to understand what happens step by step," says Doug Whittington, vice president of the Cambridge, Mass., company. "People who build real-time systems need to squeeze out every last bit of performance—and that is impossible without source code." The company will respond to reports of bugs in the original code and "will be more than happy to talk to people who have problems with their modified code," he adds.

Csharp's five system tools are highly compatible but can be used separately. They can benefit programmers involved in laboratory data acquisition, robotics, process control, and interactive graphics, among other applications.

"We feel that most of the existing software for laboratory control is much too extensive and tries to do too much," Whittington says. "And the other software provides services in a black box, where programmers cannot get at it. We provide a low-cost open system that does not try to do too much, so programmers get good performance even in a high-level language."

Most of the five tools—modules for event declarations, graphics, routine dispatching, procedure scheduling, and state-system notation—are independent of the processor and will run under many operating sys-

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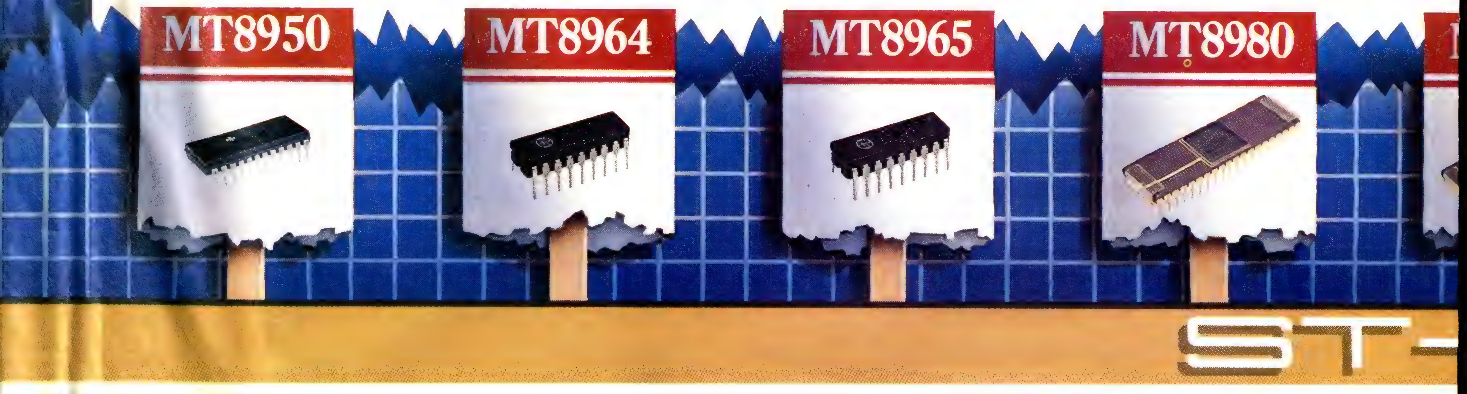

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tems, including RT11 and AT&T Bell Laboratories' Unix. Programmers can tailor their Csharp Realtime Toolkit to meet performance and memory requirements.

Programmers who deal with multiple system configurations, real-time control systems, or interactive graphics will rely on Cevent, a high-level interface to such external events as switch closures and button presses. Cevent can count and time these events.

Portable. Moreover, programmers need not rewrite application software for new hardware configurations or devices. Using Cevent, they can later enable, disable, and track events independently of a particular hardware or software implementation.

Another tool, Cgraph, permits C programmers to write portable graphics programs and to configure all of a graphics system's parameters dynamically using C procedure calls.

Cgraph works on virtually any graphics device, eliminating the need for rewriting. Programmers can create and change graphics-device defaults and parameters for a specific environment. Cgraph routines can be used as the foundation for more elaborate graphics and application packages, or they can be combined with other modules to create real-time graphics-display programs.

Providing high-level access to machine-level features like processor-priority control and device interrupts, the Cisr tool contains procedures that have been written both in assembly language and C and that access critical processor features.

Unlike Cvent and Cgraph, Cisr is processor- and often compiler-specific. The Systems Guild currently supports several microprocessors, including the 8086 and 8088, as well as the PDP-11 family. Cisr gives programmers access to the microprocessor's features without an intervening operating system; it is also particularly useful in developing tailored read-only-memory-based software.

A prioritized real-time scheduler, Csched controls the real-time execution of user procedures written in C. With it, programmers can schedule, cancel, and synchronize the execution of C procedures. In Csched's multitasking environment, each scheduled procedure can run to completion unless interrupted by a procedure with a higher priority. Complicated message passing between tasks is replaced by simple access to shared data in memory.

Watchdog. Typically, Csched can be used for asynchronous collection, analysis, and display of data in process-control or laboratory applications. It can also be used for watchdog and timing tasks in interactive programs, the company says.

The fifth tool, Cstate, provides structured process control through the use of state-system notation: a connected graph of states describing actions to be performed when a state is entered, plus conditions for changing from one state to another. The

The MT8950 Data Codec
interfaces slow speed data at up to 19.2 Kbps (e.g. RS232) to a 64 Kbps TDM channel format (ST-BUS).

The MT8964/65 PCM Filter/Codecs
perform A/D conversion in either A-Law or μ-Law. Available in 18 pin DIPs, these ICs offer advanced system control capabilities for PABX and wider applications.

The MT8980/81 Digital Time/Space Switch ICs
are non-blocking matrices that switch PCM encoded voice and/or data at 64 Kbps/channel. The MT8980 matrix is 256 × 256 channels and the MT8981 matrix is 128 × 128. Both ICs are in 40 pin DIPs.

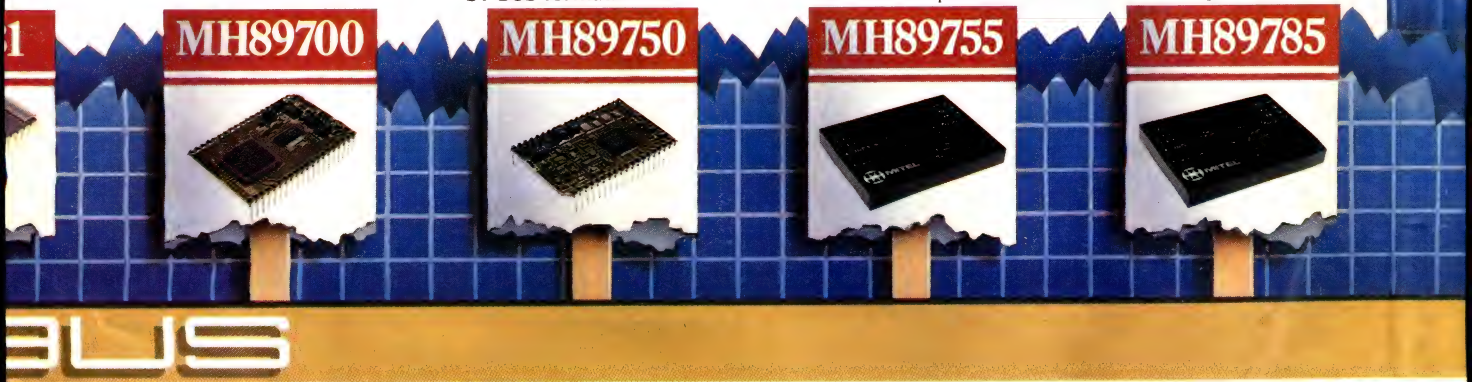
The MH89700 Digital Line Interface Module
performs full-duplex digital line interfacing at 256 Kbps over 2-pair common telephone cable. It offers user access via an 8-bit parallel I/O interface or by the ST-BUS, and is compatible with 6800 and 68000 microprocessor series.

The MH89750 T1 Digital Trunk Interface Module
performs 2-way conversion between the T1 digital trunk format (1.544 Mbps) and the ST-BUS format.

The MH89755* T1 Digital Trunk Interface Module
has all the power of the MH89750 with the addition of a high speed, 8-bit parallel I/O.

The MH89785* CCITT Digital Trunk Interface Module
performs 2-way conversion between the CCITT digital trunk format and the ST-BUS format or a high speed 8-bit parallel I/O.

Mitel Semiconductor uses ISO-CMOS and thick-film hybrid processes to produce compact and reliable ST-BUS compatible components in a variety of forms. Low power consumption and simplified power requirements are ST-BUS family traits.



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actions and conditions are represented by C procedures.

Programmers can use Cstate to simulate, analyze, or control systems with multiple discrete states, such as process control and laboratory data-collection systems. State systems, the Systems Guild points out, can be applied to many areas, including natural-language processing, stepping-motor control, compiler technology, and biobehavioral experimentation.

Available now, the source-code license sells for $600 for all five modules. Royalty fees are negotiable in the range of 10% to 20% of source-code licensing.

Systems Guild Inc., P. O. Box 1085, Cambridge, Mass. 02142. Phone (617) 451-8479 [Circle 340]

Graphics work station uses two 68000s, can be linked in multiuser configurations

Taking advantage of the performance of dual 32-bit 10-MHz 68000 microprocessors, a stand-alone graphics work station provides interactive computer-aided-design capabilities for architects, engineers, and builders. The system 25, from CalComp of Anaheim, Calif., can also be organized into multiuser and mainframe-computer-based configurations.

Two modules make up the system 25: the interactive design station and the picture-processor cabinet. In the interactive design unit, the 68000 processors execute software commands, retrieve drawings from memory, and store and print them while managing work-station peripherals. These include disks, streaming tape drives, plotters, printers, and terminals. Along with the 68000s, the interactive station holds 1 megabyte of memory, a similar capacity on floppy-disk drives, a 20-megabyte Winchester disk drive, three RS-232-C serial ports, and eight Multibus ports for expansion.

Two displays. The picture-processing module uses proprietary CalComp microprocessor-based hardware to relieve the interactive processor from the time-consuming task of display manipulation. Each station has two displays: a main high-resolution screen and a 12-in. alphanumeric screen for issuing operator prompts and messages so that operations on the main screen are not interrupted. The user can opt for either a raster 19-in.-color or 20-in.-monochrome screen. The color display has a resolution of 832 by 624 picture elements; the monochrome's resolution is 1,024 by 768 pixels.

A joystick controls the pen and zoom of the graphics image, displaying drawing information and allowing the operator to view close-ups or the entire image. A digitizer tablet and stylus are also provided with the basic station.

With the Multibus interface, users can connect the system 25 directly to a Digital Equipment Corp. VAX computer for mass storage and centralizing computer operations. Introduced at the National Computer Graphics Association conference earlier this month in Anaheim, Calif., the new system will be ready for shipment in June.

Pricing for a basic configuration starts at $65,000, which includes software, installation, and a training program.

CalComp, 2411 W. La Palma Ave., P. O. Box 3250, Anaheim, Calif. 92803. Phone (714) 821-2080 [Circle 342]

Acquisition system has no pots to trim

The screwdriver used to calibrate the variable low-level analog-input portion of data-acquisition systems may soon join the slide rule in engineering's trash bin. The reason is a programmable subsystem from Neff Instrument Corp., Monrovia, Calif., that simplifies calibration and also upgrades overall performance of data-acquisition equipment.

Usually, every channel in the amplifier and analog-to-digital section of these systems (including those made by Neff) requires numerous adjustment potentiometers that have to be continually calibrated "to get rid of zero and gain errors," says James T. Barber, marketing manager. Otherwise, the accumulated noise and common-mode-rejection errors can affect the accuracy of the channels—there often being hundreds in a large system—even to the point of stopping the operation completely.

The Neff series 600 front-end subsystem eliminates the potentiometers and replaces them with a calibration relay for each channel, plus an on-

board microcomputer that controls them and the entire unit. On command, the computer checks an internal reference-voltage source and then adjusts the zero and gain of each channel within the basic system accuracy of ±0.02% of full scale, ±2 μV. Moreover, this accuracy, which Barber bills as "the highest yet for data acquisition," is guaranteed for one year entirely through the automatic calibration.

Second goal. But eliminating the potentiometers, while noteworthy since it marks the end of conventional manual calibration, is only one benefit of Neff's 2½-year upgrading effort. A more ambitious goal is to simplify data-acquisition systems and stimulate interest in equipment that Barber describes as "horribly complicated, even for engineers close to it." Typically, voluminous specifications often conflict, overlap, and generally confuse everyone, he says. Therefore, Neff presents the performance in a single system-accuracy figure and offers much automation.

Thus, each channel has programmable gain and filter frequency, in 12 binary steps over a range from ±5 mV to ±10.24 V full scale. Also, the series 600 has 16-bit resolution and a sample rate up to 100 kHz, double the previous rate of front ends in Neff's system 620, on the market for several years.

The automatic calibration serves also as a diagnostic test of system operation; with it, a user knows the system is ready to go. Standard interfaces are available for major models of minicomputers.

An advantage is that the combined programmable and calibration features allow a data-acquisition system to continue operating as they are being performed. "There are some big test configurations, for example, that have schedules that [don't permit them] to go down," notes Barber.

Another feature of the series 600 is continuous analog outputs from each channel, a result of Neff's amplifier-per-channel approach. Available at the rear panel, these outputs at ±5 mA, are unaffected by filters, multiplexers, or post amplifiers.

Other specifications include a gain stability of ±0.002% of full scale/°C change from the auto-calibration temperature; an operating common-mode voltage of ±10 V dc or ac peak; and a nondamaging input overload of ±100 V dc or ac peak common mode or normal mode. Static crosstalk is said to be 120 dB, and dynamic crosstalk is specified at ±0.01% plus 0.0025× the post amplifier gain at 100 kHz.

Neff will begin shipping the new units in June, priced at $700 per channel for smaller equipment, down to $500 per channel for multichannel configurations.

Neff Instrument Corp., 700 S. Myrtle Ave., Monrovia, Calif. 91016. Phone (213) 357-2281 [Circle 341]

Low-cost IC controls brushless dc motors

A controller from LSI Computer Systems provides commutation control of three-phase brushless dc motors where absolute precision is not essential, and at a price that suits the unit for relatively inexpensive applications. Brushless dc motors have distinct advantages over conventional dc motors—most notably, the fact that they last almost indefinitely and do not generate sparks. But they also can require complex and costly electronics to distribute current to the windings. At $1.70 each in quantities of 1,000, the LS7261 is intended to overcome that drawback.

Typical applications might include open-loop control for oil burners, compressors, and similar products—any of which might need a motor that operates continuously, says Ron Colino, marketing vice president. Brushless motors do not need frequent servicing and can be used safely in a potentially dangerous area. With direct current, their speed can vary constantly, an important factor in air-conditioning systems.

Long-lived. The LS7261 controller sacrifices the precision needed for heavy-duty applications in favor of durability and low cost. Built around a monolithic, ion-implanted p-channel MOS circuit, it responds to signal changes coming from the motor-position sensors to provide electronic commutation of the motor windings.

Duty-cycle modulation of outputs for motor-speed control is accomplished through either the enable input or the analog input pins in conjunction with the signal from the oscillator. Overcurrent circuitry protects the windings, associated drivers, and power supply. A positive braking feature makes possible rapid deceleration.

LSI chose p-MOS because of its greater voltage tolerance (operation from 7 to 28 V dc) and durability as compared with complementary-MOS. Noise sensitivity is reported not to be a problem. In addition, the cost savings over C-MOS are substantial because there is no need for auxiliary drivers to amplify voltage at the range's higher end.

The 7261 also includes externally selectable input-to-output codes for 60/120/240/360° electrical sensor spacing; analog speed-control input; forward/reverse control; and six dc outputs.

LSI Computer Systems Inc., 1235 Walt Whitman Rd., Melville, N. Y. 11747. Phone (516) 271-0400 [Circle 344]

Computers & peripherals

Page printer is fast, mixes text, graphics

Capable of producing publication-quality graphics and documentation, the Imagen 5/480 nonimpact laser page-printing system aims at increasing efficiency and lowering costs. The printer can mix text and graphics on a single page and prints at a rate of 5 pages/min, with a resolution of 480 dots/in. It can also mix several font styles and sizes on one line of text.

Another unit recently introduced, the Imagen 8/300—a desktop page printer that costs less than $10,000—can print 8 pages/min at a resolution of 300 dots/in. With a noise level of 55 dBa, it works more quietly than typical impact printers do.

Available now, both printers have been designed to work with many host computers running under AT&T Bell Laboratories' Unix operating system and using such document-composition systems as troff, TeX, and Scribe. Model 5/480 costs less than $20,000; the 8/300 costs $9,950.

Imagen Corp., 2660 Marine Way, Mountain View, Calif. 94043. Phone (415) 496-2100
[Circle reader service number 361]

Multiuser architecture now supports 16-bit processor cards

Molecular Computer Corp. has configured its local-network-in-a-box multiuser architecture to include both 16- and 8-bit processors. The computer now supports a total of five operating systems capable of sharing files with one another. The series 9 includes application-processor boards built around the 8-bit Z80A and the 16-bit 80186, and each board has 256-K bytes of memory. Users can run programs under MS-DOS and four versions of CP/M (8- and 16-bit, single and multiuser).

The basic series 9000 has slots for as many as nine application-processor boards and includes a Z80-based file-processor board. The processors and the peripherals are linked by the company's proprietary m/Bus, which is a 400-K-byte/s carrier-sense, multiple-access contention bus with collision detection.

Each user has a dedicated processor board and dedicated memory. Frequent users can automatically be assigned to their preferred processors at log-on, but any user can access any of the boards, and a single user can use all of them concurrently.

The series 9 supports nine application processors in its base system cabinet and has slots for a 20- or 40-megabyte 5¼-in. Winchester disk drive and a 360-K-byte floppy drive. An expansion cabinet with slots for nine additional application processors and two additional disk drives is available.

The system now links MS-DOS and CP/M files by putting all MS-DOS files, which are hierarchical, into a single large CP/M file. Within 90 days, Molecular will have software drivers that dynamically map each type of file into the other format. The series 9 system, available now, costs $7,995 with a 20-megabyte hard-disk drive and $9,995 with a 40-megabyte hard-disk drive. Additional 16-bit application processors list for $1,695, 8-bit application processors for $995. The concentrator unit priced at $1,995.

Molecular Computer Corp., 251 River Oaks Pkwy., San Jose, Calif. 95134. Phone (408) 262-2122 [Circle 368]

32-bit engineering computers operate alone or in networks

The CDS 3000 series is a line of fully configured and packaged 32-bit work stations intended for use in stand-alone or networked design and engineering applications. Based on the 68010 processor, the CDS 3000 incorporates AT&T Bell Laboratories' Unix operating system and features personal-management tools, including a report generator and a data-base manager with an interactive data-query language.

A second work station, the CDS 5000, built up from the existing CDS 4000, is a high-end system for controlling large amounts of manufacturing, construction, and engineering data and for providing links to corporate data bases. It can control and manage more than 40 gigabytes of graphical and nongraphical data. Incorporating the VM/CMS operating system and the SQL/DS relational data-base system, the CDS 5000 uses the IBM 4300 processor.

Volume shipments of both the CDS 3000 and 5000 systems will begin in the fourth quarter. CDS 3000 systems range in cost from $35,000, for a CDS 3310 networked desktop work station, to $52,000, for a CDS 3411 stand-alone suited for production environments. The cost of upgrading currently installed CDS 4000 systems to the CDS 5000 ranges from $485,000 to $650,000.

Computervision Corp., 100 Crosby Dr., Bedford, Mass. 01730. Phone (617) 257-1800
[Circle 362]

Fault-tolerant system triples its predecessor's performance

Targeted primarily at on-line transaction-processing and communications applications, the models XA 400 and XA 600 fault-tolerant computers triple the performance range of the existing Stratus/32 product line. They are software-compatible with the company's FT 200, and any combination of the three models can form a system capable of executing thousands of transactions a second.

The model XA 400 uses four independent Motorola 68010 processors, all of which can run a different program. The model XA 600 uses six independent 68010s, each accelerated by dedicated cache memory and a hardware arithmetic processor providing commercial (fixed-decimal) arithmetic.

Available now, the XA 600 costs $270,000; when available in October, the XA 400 will sell for $185,000.

Stratus Computer Inc., 17 Strathmore Rd., Natick, Mass. 01760. Phone (617) 653-1466
[Circle 363]

Systems integration

Controller puts Multibus units on Ethernet

The NI3210 controller board provides Multibus-based systems with a link-level connection to the standard Ethernet/IEEE 802.3 local network. With both a dual-port random-access memory and an on-board direct-memory-access controller, the board offers a throughput rate of 10 Mb/s while minimizing the service load placed on the host Multibus.

For efficient handling of Ethernet packets varying in length from 64 to 1,518 bytes, the NI3210 uses linked-list buffer management to chain small packets together. For Multibus host systems that organize their odd and even data bytes in the reverse of the way required by their transmission protocol, it includes a programmable byte-swap facility that re-orders the data bytes as they transfer to and from the controller.

A protocol package written in C—the NS4244 XNS Internet Transport Protocols for Unix System V—offers a transport system for one or more user-written application programs when used with the NI3210.

Available now, the NI3210 sells for $760 in quantities of 100. Binary licenses for the software start at $200 per copy.

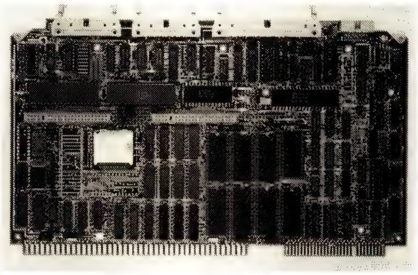
Interlan Inc., 3 Lyberty Way, Westford, Mass. 01886. Phone (617) 692-3900 [Circle reader service number 391]

Trio of computer boards run under iRMX; two use the 80186

Based on the iAPX 186 and iAPX 86 microprocessors, the general-purpose iSBC 186/03 and iSBC 86/35 and the graphics-oriented iSBC 186/78 single-board computers integrate operating-system functions, a central processor, peripheral-device interfaces, memory, and software on 6.75-in.-by-12-in. cards. Each can replace several conventional boards and, compared with other single-board systems, has faster processing speeds, lower total-system costs, and reduced power requirements, the company says.

The three run under iRMX operating-system software. They are meant for use in such areas as computer-aided design, industrial control, robotics, and office systems.

The 186/03 is available now at a price of $1,650. Engineering samples of the 186/78 will be available in June and will sell for $3,000. The 86/35, available now, sells for $3,495. When 256-K chips become available, the board will hold as much as 1 megabyte of memory.



Intel Corp., Literature Dept. C-21, 3065 Bowers Ave., Santa Clara, Calif. 95051 [Circle 392]

VMEbus CPUs with 68000s suit industrial-control tasks

Targeted for industrial applications, a pair of central processing units are built on VMEbus cards. They are based on 68000 microprocessors.

The model CPU-1B, compatible with VMEbus Revision B, is available with an 8- or 10-MHz processor and can hold 128- or 512-K bytes of dynamic random-access memory. It features a 24-bit programmable timer, a real-time clock with battery, and sockets for 128-K bytes of erasable programmable read-only memory or up to 16-K bytes of static RAM.

Designed to hold as much as 1 megabyte of memory, the CPU-2 is a densely packed multiprocessor board that comes with either the 68000 or 68010 processor. The CPU-2 will be configured to the user's specifications with an 8- or 10-MHz processor and a dynamic RAM of 128-, 156-, or 512-K bytes, or 1 megabyte. The CPU-2 comes with such options as support circuits for up to four 5¼-in. floppy-disk drives and a communications controller.

Available now with quantity discounts, the CPU-1B is priced at $1,295, the CPU-2 at $1,795.

Force Computers Inc., 2041 Mission College Blvd., Santa Clara, Calif. 95054. Phone (408) 988-8686 [Circle 394]

Fast disk controller handles SCSI bus and SMD drives

The ACB-5580 hard-disk controller board, which supports up to seven host central processing units through the Small Computer Systems Interface (SCSI) bus and up to four Storage Module Drive (SMD) disk drives, maximizes the input/output performance of multitasking microcomputers. The board can control either 8- or 14-in. SMD disk drives.

The controller includes features of the company's ACB-5500 board for 5¼-in. Winchester disk drives, among them disconnect/reconnect, and file sharing. Thanks to the controller's bus disconnect/reconnect function, a computer can run concurrent I/O tasks by handling multiple seeks and reads and writes with the I/O bus disconnected from the processor; it reconnects only when a drive has data ready to be read or written.

The controllers feature noninterleaved operation, an advantage over competing units needing four or more disk rotations in interleaved operation to access all information on a single track. Also, the company has developed two intelligent host adapters, which improve system performance by functioning as I/O processors working with the operating system's I/O supervisor.

Samples of the AHA-5580, priced at $980, come out in June. Production begins in the third quarter.

Adaptec Inc., 580 Cottonwood Dr., Milpitas, Calif. 95035. Phone (408) 946-8600 [Circle 396]

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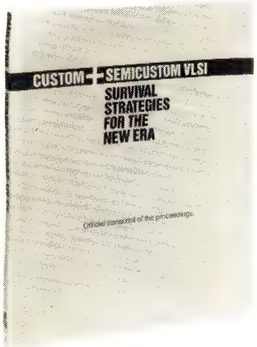

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Microcomputers & systems

LSI-11 mimic is flexible and runs Unix

Model 40, an LSI-11-compatible computer system with many software, disk-drive, memory, and processor options, can be arranged in 155 ways. It can run all system and application software developed for the LSI-11/23 and LSI-11/73 central processing units and can do so without modification.

The key to the system's flexibility is what the company calls a foundation architecture, which includes a system enclosure, a choice of fixed and removable peripherals, and LSI-11 processors and memory. All system components are combined on one four-layer printed-circuit board that includes the mass-storage-device controller, two serial communications ports, all backplane circuitry, and the hardware to operate the support-monitor subsystem.

A comparable LSI-11 from DEC would take three boards and use up three Q-bus backplane slots. The foundation module, as the board is called, does not even use a slot; it is larger than Q-bus cards and lies beside the Q-bus backplane, within the system enclosure. Although the foundation module is not itself a Q-bus card, it is connected to the Q bus, and any LSI or LSI-compatible card, such as DEC's DLVII-J or DZV-11 four-port modules, can be used in the backplane and operate in the system.

What's more, up to four mass-storage peripherals—different variations of 5¼- and 8-in. floppies, 5¼-in. Winchesters, and a start/stop cartridge-tape subsystem—can be configured without taking up any bus slots. The company says that model 40 has more peripheral devices in a single 5¼-in. enclosure than any other DEC-compatible microcomputer on the market yet still provides a full-size backplane for expansion.

The support-monitor subsystem, also included in the foundation module, contains software and hardware used for system status analysis, system utilities, and diagnostics. Model 40 supports high-performance, real-time, and time-sharing operating systems, including RT-11, RSX-11M, RSX-11M-Plus, RSTS/E, Unix, and TSX-Plus.

Prices start at $5,800 and delivery takes about eight weeks.

Scientific Micro Systems Inc., 777 East Middlefield Rd., Mountain View, Calif. 94043. Phone (415) 964-5700 [Circle reader service number 407]

Engineering system integrates a test station and the IBM PC

The model PC7 development work station, which links the Step-7 firmware-integration test station with International Business Machines Corp.'s Personal Computer, simplifies the work of development engineers. The work station requires only system commands associated with the MS-DOS operating system.

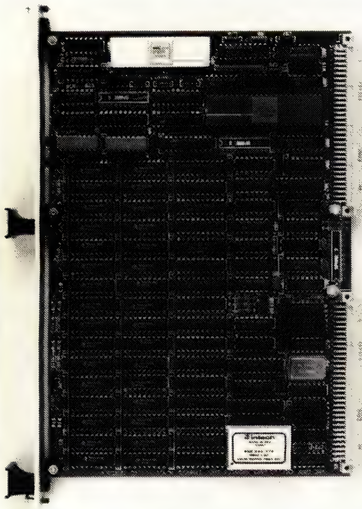
Integrating the PC7 and a PC makes it possible to define bit-slice designs, to assemble programs, to format object code, and to debug microcode. With this versatility, a design-engineering laboratory can create work stations dedicated to developing high-speed microprocessors. In addition, the PC7 puts often-used disk files on the PC's RAM, which reduces file access time and promotes better operator-response time.

With the PC-interface capability,

the Step-7 costs from $10,000 to $25,000, depending on software ordered. Deliveries are within 30 days.
Step Engineering, 757 Pastoria, Sunnyvale, Calif. 94088. Phone (408) 733-7837
[Circle 403]

Controller produces display of 16 colors, 600 by 800 pixels

The IV-1651 bit-mapped graphics-display controller produces a 16-color display with a resolution of up to 600 by 800 picture elements or a 4-color display with resolutions of 1,024 by 1,024 or 1,280 by 768 pixels. Its features include a hardware pixel processor that can plot vectors and arcs at 800 ns/pixel, integer zoom, and a direct-memory-access port for rapid screen updates.



An optional hybrid provides a color-translation table and three video digital-to-analog converters to allow displays of 16 colors from a pallette of 4,096. The IV-1651 can also be applied in an eight-color mode with the fourth image-plane memory used to provide either a blink attribute or a white overlay.

Available now, the IV-1651 is priced at $1,995 with 128-K bytes of display memory and at $2,295 with 256-K bytes of display memory.
Ironics Inc., 117 Eastern Heights Dr., P.O. Box 356, Ithaca, N. Y. 14805. Phone (607) 277-4060
[Circle 402]

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Components

Data separator incorporates PLL circuitry

Fabricated using a standard bipolar advanced low-power Schottky process, a monolithic data-separator chip incorporates on-board phase-locked-loop control circuitry. The model DP8460 is designed for use in 3.5-, 5.25-, 8-, and 14-in. hard-disk drives, high-density floppy-disk drives, and optical-disk drives. It can be implemented in either the drive or controller section of the disk system.

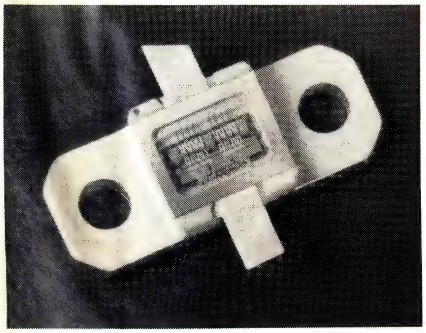
The company says that the use of a PLL function along with a process-insensitive delay line lets the chip tolerate more bit jigger than other systems can. Also, the DP8460 requires no trimming and will not drift, resulting in more accurate and reliable signal transmission.

Available in a 24-pin dual in-line package, the 8-ns version is priced from $25.75 and up when purchased in quantities of 100 to 999. Prototypes can be delivered in four weeks.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 721-5000 [Circle reader service number 371]

Emitter-plate-metal technology keeps S-band transistor stable

Intended for military and commercial radar/transponder applications in the 2.7-to-3.5-GHz frequency range, a line of S-band pulsed power transistors with power levels of 55 W minimum incorporates a design technology called emitter-plate-metal, which can improve broadband ability and stability at these frequencies, according to the company.



The MSC AM 83135-50 produces more than 50 W of power over a 400-MHz bandwidth, while the AM 82931-55, specified at 55 W minimum, typically delivers 60 to 65 W of peak power over the 2.9-to-3.1-GHz range. The series has been fully characterized for phase tracking, pushing, and linearity. Uniformity and reproducibility are ensured by in-process controls, ion-implanted vertical impurity profiles, quasi-integrated internal impedance-matching circuitry, and fully automatic wire bonding. The devices are enclosed in a fully hermetic, MIL-qualified, solder-sealed package designed for use in harsh environmental conditions.

The products are available within eight weeks. Both the 83135-50 and the 82931-55 cost about $500 each when ordered in quantities of 100.

Microwave Semiconductor Corp., 100 School House Rd., Somerset, N. J. 08873. Phone (201) 469-3311 [Circle 378]

MOS VLSI circuit combines most CRT-controller functions

Combining virtually all the functions of a cathode-ray-tube controller on one MOS very large-scale integrated circuit, a pair of video-terminal logic controllers provide a video-timing generator and controller, character generator, graphics generator, video-attribute controller, video-shift register, and memory controller.

The CRT 9028 is designed to interface with the 8085, Z80, 8051, and 6500/6800, as well as similar microprocessors and microcomputers. The CRT 9128 is for use with the 8086, 68000, and Z8 processors. By providing complete display and memory control, as well as a direct microprocessor interface, the CRT 9028 and 9128 allow the construction of complete CRT terminals with as few as six integrated circuits. Both controller chips provide 32-, 64-, and 80-column displays with up to 25 data rows.

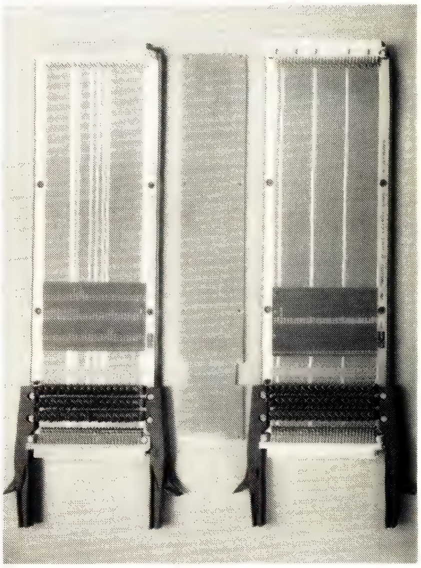
Samples of both controllers are available from stock in ceramic or plastic packages at a 100-piece price of $22.50 apiece.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, N. Y. 11788. Phone (516) 273-3100 [Circle 373]

VMEbus extender boards have full ground planes

Engineered to the same parameters as the firm's high-speed VMEbus backplanes, the J1 and J2 VMEbus extender boards have a three-layer construction and provide signal paths with 0-V guard-track protection and a full ground plane.

By removing the jumper links supplied with each board, the power and signal tracks can be interrogated for diagnostic purposes. A logic analyzer can be connected to the board if a Type-C DIN connector is attached to it. Any combination of J1 and J2 extenders can be assembled to a double-height format using a conversion kit that can be bolted to the board.



At a price of $243 each, the J1 and J2 boards can be delivered from stock.

BICC-Vero Electronics Inc., 171 Bridge Rd., Hauppauge, N. Y. 11788. Phone (516) 234-0400 [Circle 376]

Products newsletter

Package automates software development

A software development and management system from Oregon Software Inc. **promises to replace manual methods with three program packages to build application code while managing the development process.** SourceTools consists of a package that controls the creation and modification of source-code files, a file rebuilder that updates programs as to component changes, and a package that maintains parallel files on the host and target-development systems. The Portland, Ore., firm's system is now available for use on Digital Equipment Corp.'s PDP-11 and VAX computers. The price for the RSX operating-system version is $4,500. The RSTS operating-system version sells for $3,600.

Disk drive, more memory enhance IBM's PCjr

Those who have resisted the International Business Machines Corp. PCjr because of a lack of features may soon pick one up, thanks to an expansion kit from Rapport Corp., available now. Called the Drive Two Enhancement Package, the North Salt Lake City, Utah, firm's kit includes a 360-K-byte floppy-disk drive, an expansion slot permitting the PCjr to hold up to 512-K bytes of memory, a parallel port, and a clock-calendar. With the $675 kit, **users can run the MS-DOS 1.1, 2.1, or 2.0 operating system** and have access to IBM Personal Computer software.

Design station gets library, logic simulation interfaces

Previously available only on larger machines like the VAX minicomputer, the Cadat logic-simulator software package from HHB Softron of Mahwah, N. J., will be adapted to FutureNet Corp.'s Dash-1 Schematic Designer. To provide the necessary computing to support the sophisticated simulator, FutureNet, of Canoga Park, Calif., will add an auxiliary processor board to the Dash-1, which is based on the IBM Personal Computer. Available on Dash-1 in September, **the Cadat will provide complete simulation support for a logic design from its inception through the generation of a manufacturing test program.** The Electro/84 show brought an announcement of a pact between FutureNet and LSI Logic Corp., Milpitas, Calif., whereby the latter's gate-array library will be made available on the Dash-1. The firms also developed an interface enabling users to design the LL3000, LL5000, and LL7000 gate arrays using the Dash-1 and to translate schematic designs to LSI Logic's logic-design system at its design centers. The library sells for $1,495.

Low-priced unit prints 72 dots/in.

A dot-matrix printer for home computers manufactured by the Smith-Corona Group of SCM Corp., New Canaan, Conn., will be on the market in July. **The $259 Fastex-80 unit, which operates at 80 characters/s, prints with horizonal resolutions of 60 and 72 dots/in. and a vertical resolution of 72 dots/in.** Using a drop-in ribbon cassette, the Fastex-80 features bit-image graphics, true descenders, and an RS-232-C interface.

Efficient 8088 processor now comes in C-MOS

Samples of the popular model 8088 16-bit processor are now available in C-MOS versions from Harris Semiconductor Digital Products, Melbourne, Fla. The model 80C88, which operates at up to 5 MHz, has static C-MOS circuitry allowing standby and low-frequency operation to be built into a system. **It requires less than 10 mA of power while operating and less than 500 μA in the standby mode.** Prices range from $48.50 for the commercial part to $252.76 for the military device.

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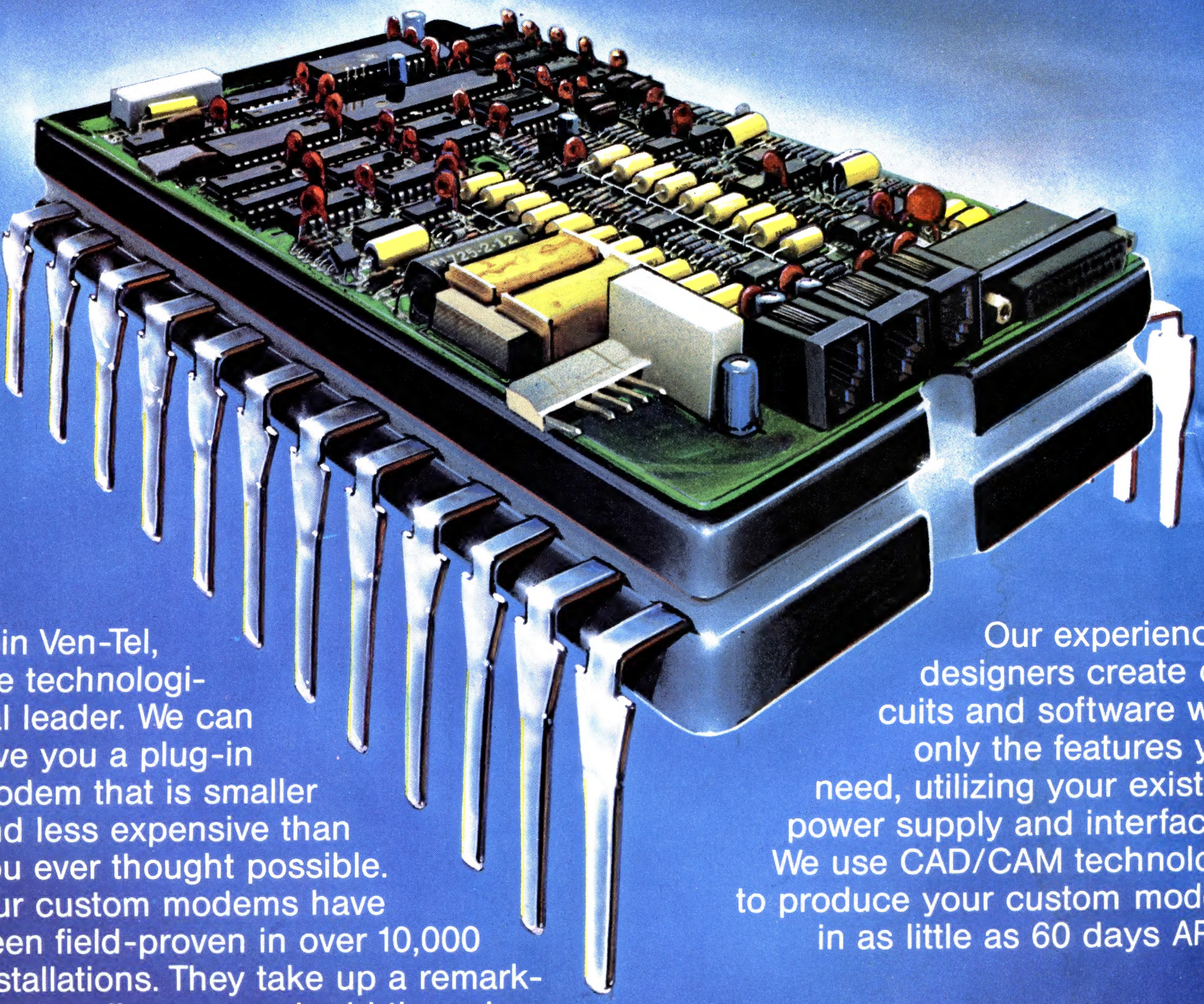

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